A Tale of Three Trends: Mask Synthesis in the Era of CL, ML and GPU

Danping Peng
Siemens EDA

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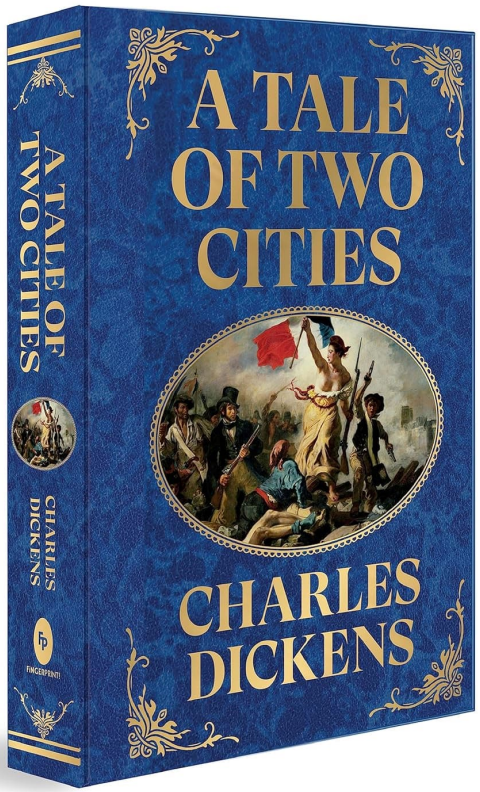
It was the best of times, it was the worst of times, it was the age of wisdom, it was the age of foolishness, it was the epoch of belief, it was the epoch of incredulity, it was the season of Light, it was the season of Darkness, it was the spring of hope, it was the winter of despair, we had everything before us, we had nothing before us, we were all going direct to Heaven, we were all going direct the other way. . . .



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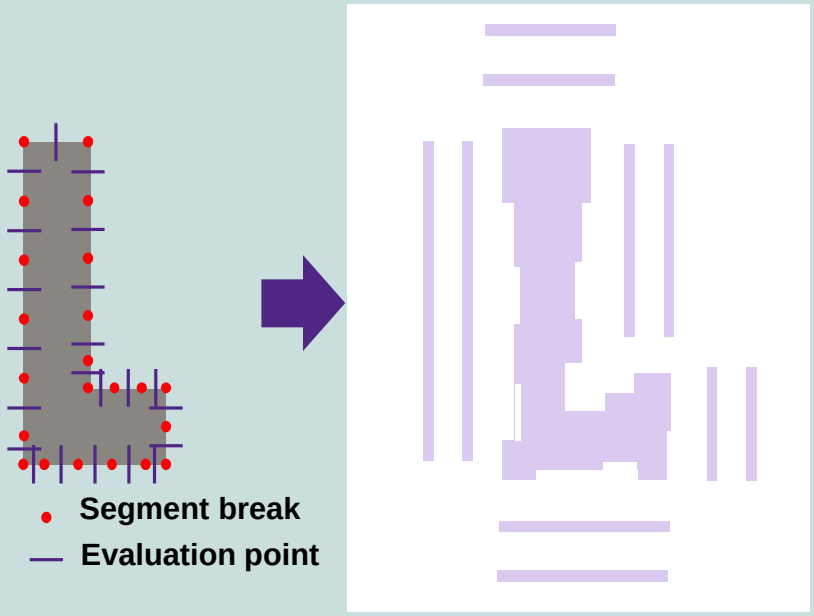
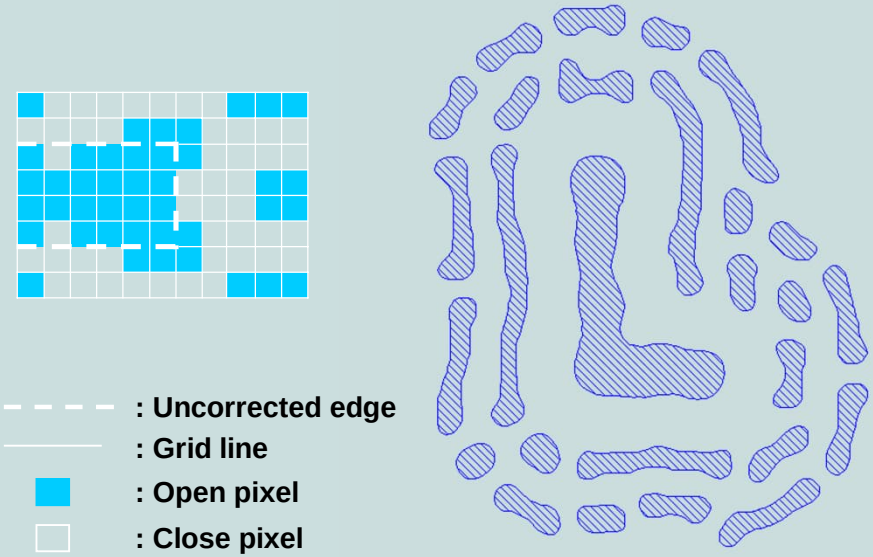
Outline of Today

- The Origins of ILT
- A Primer on Level Set ILT
- The Long Road to HVM
- ILT with Deep Learning
- Future Direction of Mask Synthesis

Conventional OPC vs ILT

Conventional OPC	Free-Form ILT





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ILT Has Been Around For Over Two Decades

Early pioneers applied inverse techniques for photonic crystals to OPC

While working on inverse techniques for photonic crystals, they thought of applying the same technique to OPC problems.

Stan Osher, UCLA

Eli Yablonovitch, UC Berkeley

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ILT Went Commercial

- Luminescent Technology, Inc. was founded in late 2002 by Stan Osher, Dan Abrams, and Jack Herrick to develop and commercialize the seminal ideas.
- Engaged with imec, Intel, TSMC and Samsung for early tape-out.

Dan Abrams
CEO

Jack Herrick
CFO

First Engineer
Later CTO

Leo Pang
SVP of Marketing

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Some Early ILT Results

US007571423B2

(12) **United States Patent**
Abrams et al.

(10) **Patent No.: US 7,571,423 B2**
(45) **Date of Patent: Aug. 4, 2009**

(54) **OPTIMIZED PHOTOMASKS FOR PHOTOLITHOGRAPHY**

(75) Inventors: **Daniel Abrams**, Palo Alto, CA (US); **Danping Peng**, Richmond, CA (US); **Stanley Osher**, Pacific Palisades, CA (US)

(73) Assignee: **Luminescent Technologies, Inc.**, Palo Alto, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 323 days.

(21) Appl. No.: **11/225,378**

(22) Filed: **Sep. 12, 2005**

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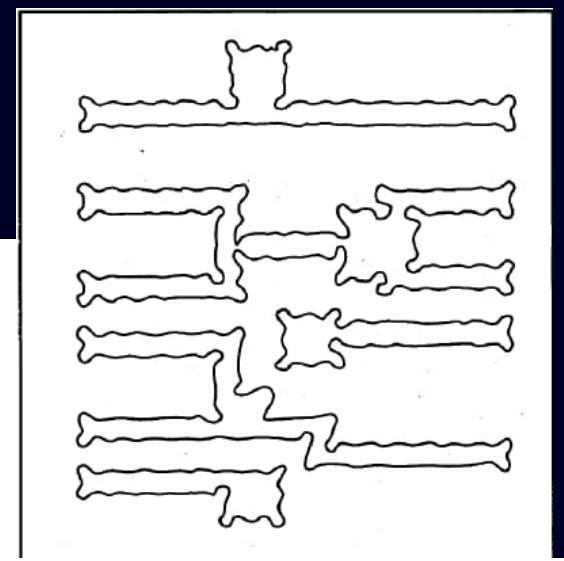
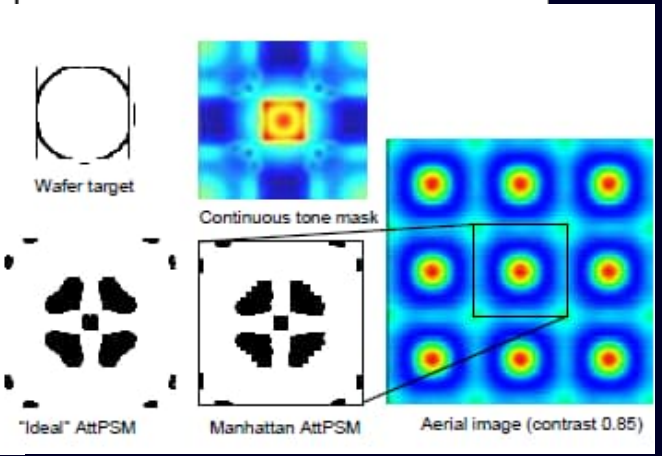
(Continued)





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ILT at Mentor Graphics - Now Siemens EDA

Seminal 2006 ILT paper by Yuri Granik with complete mathematical formalism of ILT optimization problem

Key observations of this work:

- Complete formulas (all 56 of them!)
- The term “ILT” is not used in this work
- Formal discussion of objectives, constraints, linear vs non-linear optimizations, gradient methods, computational complexity and results
- **This work formed the basis of the Mentor Graphics ILT (pxOPC product)**

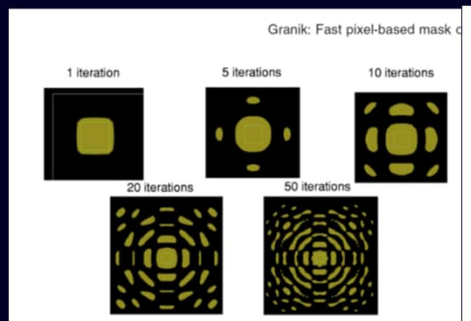

Fig. 4 Gradient-descent mask iterates are shown after 1, 5, 10, 20, and 50 iterations.

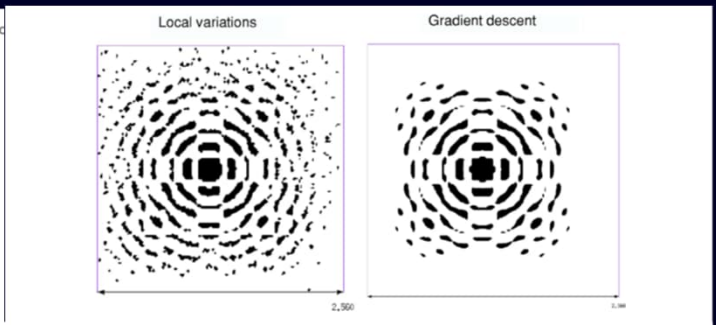

Fig. 5 Comparison between local variations and gradient-descent optimizations for the target as an isolated contact hole of 100-nm size, printed with quadrupole illumination. The mask pixels of 10-nm size are thresholded at 0.5 level (the dark areas have transmissions >0.5) and cover 2.56×2.65-μm layout area. The simulation time of gradient descent with an analytically calculated gradient is about 2 s on a SunBlade station. The solution with local variations is less regular than with the gradient descent, because the pixels are iterated randomly. Up to eight assist rings are discernable.

Fast pixel-based mask optimization for inverse lithography

Yuri Granik
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131

Abstract. The direct problem of optical microlithography is to simulate printing features on the wafer under the given mask, imaging system, and process characteristics. The goal of inverse problems is to find the best mask, imaging system, or process to print the given wafer features. In this study, we proposed the strict formalization and fast solution meth-
ods of inverse mask problems. We stated inverse mask problems (or
inversion” problems) as nonlinear, constrained minimization prob-
ver a domain of mask pixels. We considered linear, quadratic, and
ear formulations of the objective function. The linear problem is
by an enhanced version of the Nashold projections. The quadratic
m is addressed by eigenvalue decompositions and quadratic pro-
ming methods. The general nonlinear formulation is solved by the
ariations and gradient descent methods. We showed that the gra-
f the objective function can be calculated analytically through con-
ns. This is an important practical result because it enables layout
on on a large scale in order of $M \log M$ operations for M pixels.
Society of Photo-Optical Instrumentation Engineers. [DOI: 10.1117/1.2399537]

terms: optical lithography; optical proximity correction; OPC; illuminator
ation; resolution enhancement techniques; RET.
05068RR received Sep. 22, 2005; revised manuscript received Aug. 14,
ccepted for publication Aug. 21, 2006; published online Dec. 13, 2006.

Fig. 10 Examples of layout inversion for the random logic and static random access memory cell.

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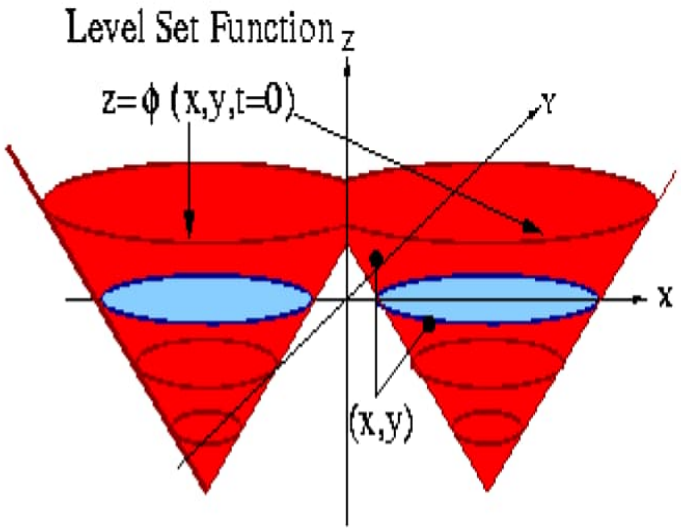
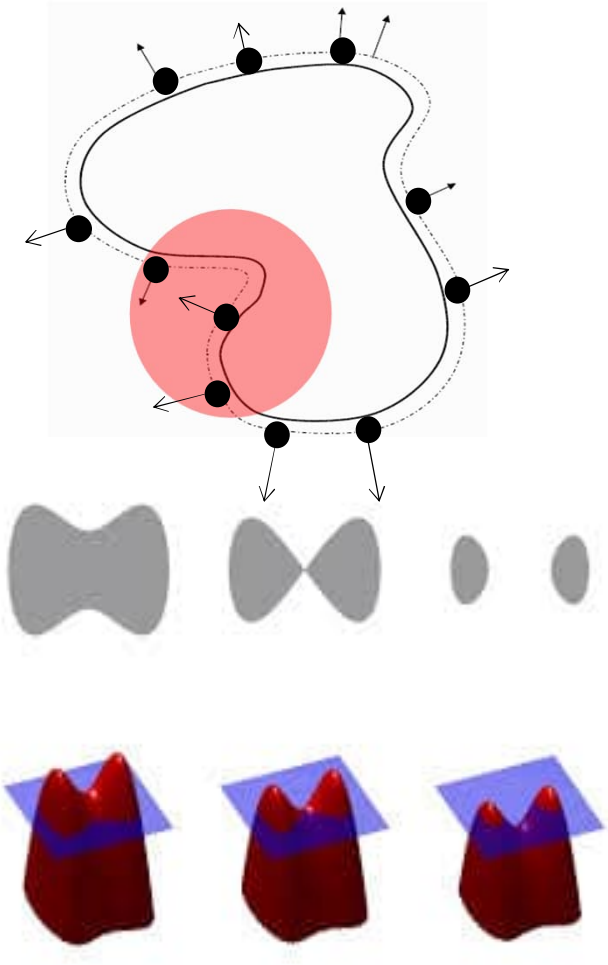
What is Level Set Method?





Represent 2D contour as the level-set of a 3D Surface!

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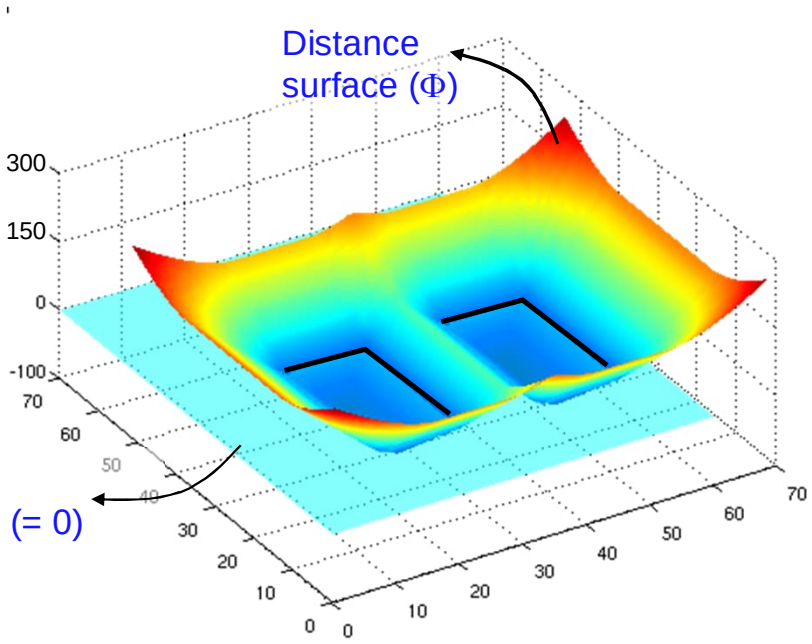
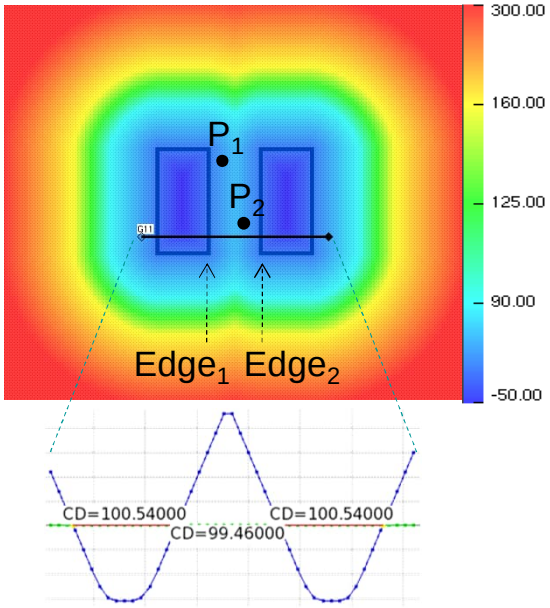
Level-set Is Key Enabler Of Freeform Mask Correction

- A mask representation scheme that describes a 2D-mask as the contour of a 3D surface
- The 3D surface value represents the distance a given point is to its closest mask edge



Mask Edge
Threshold level (= 0)

The closest edge of P_1 is $edge_1$
The closest edge of P_2 is $edge_2$



Source: Peng DAC 2021

Threshold = 0

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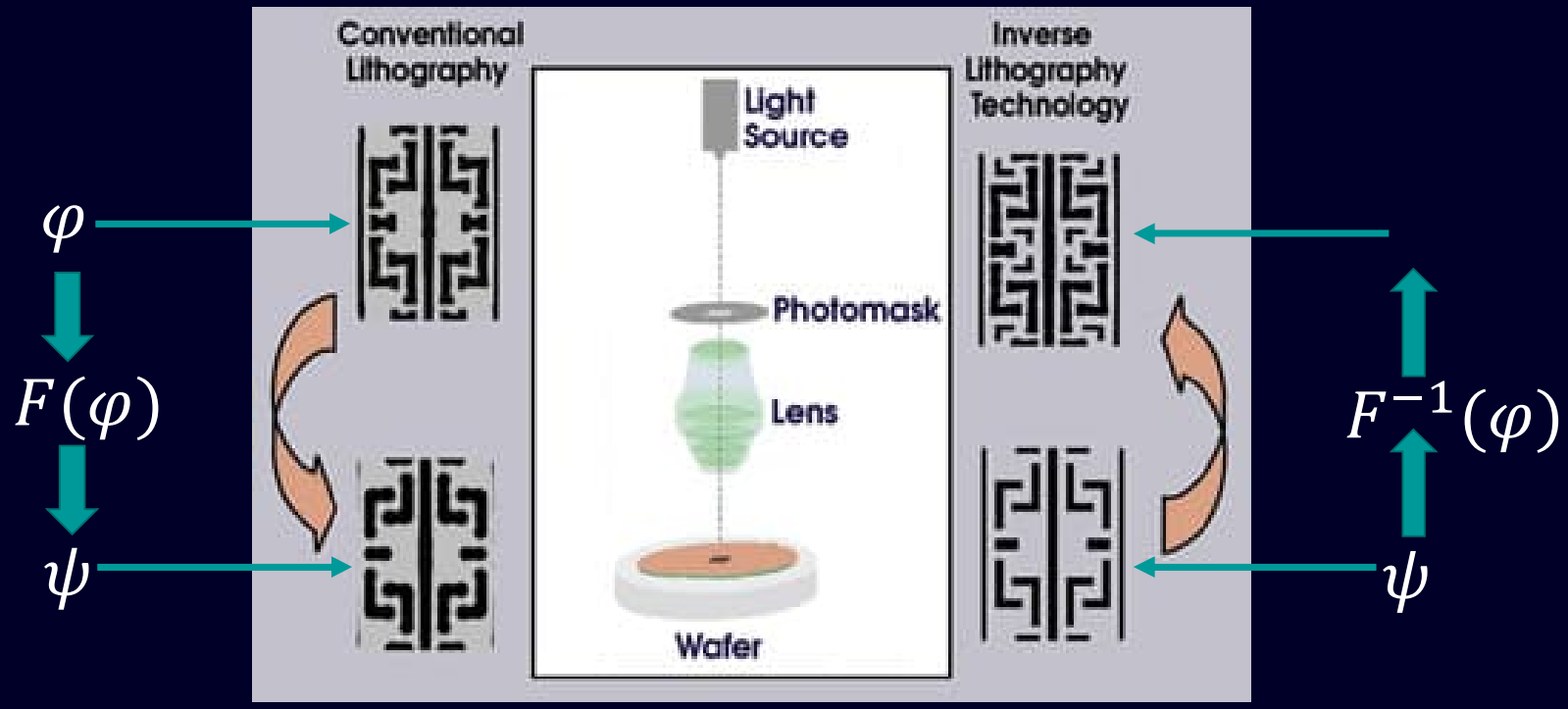
What is Inverse Lithography Technology (ILT)?

$$H(\varphi) = \iint |F(\varphi) - \psi|^2 \mathrm{dxdy}$$



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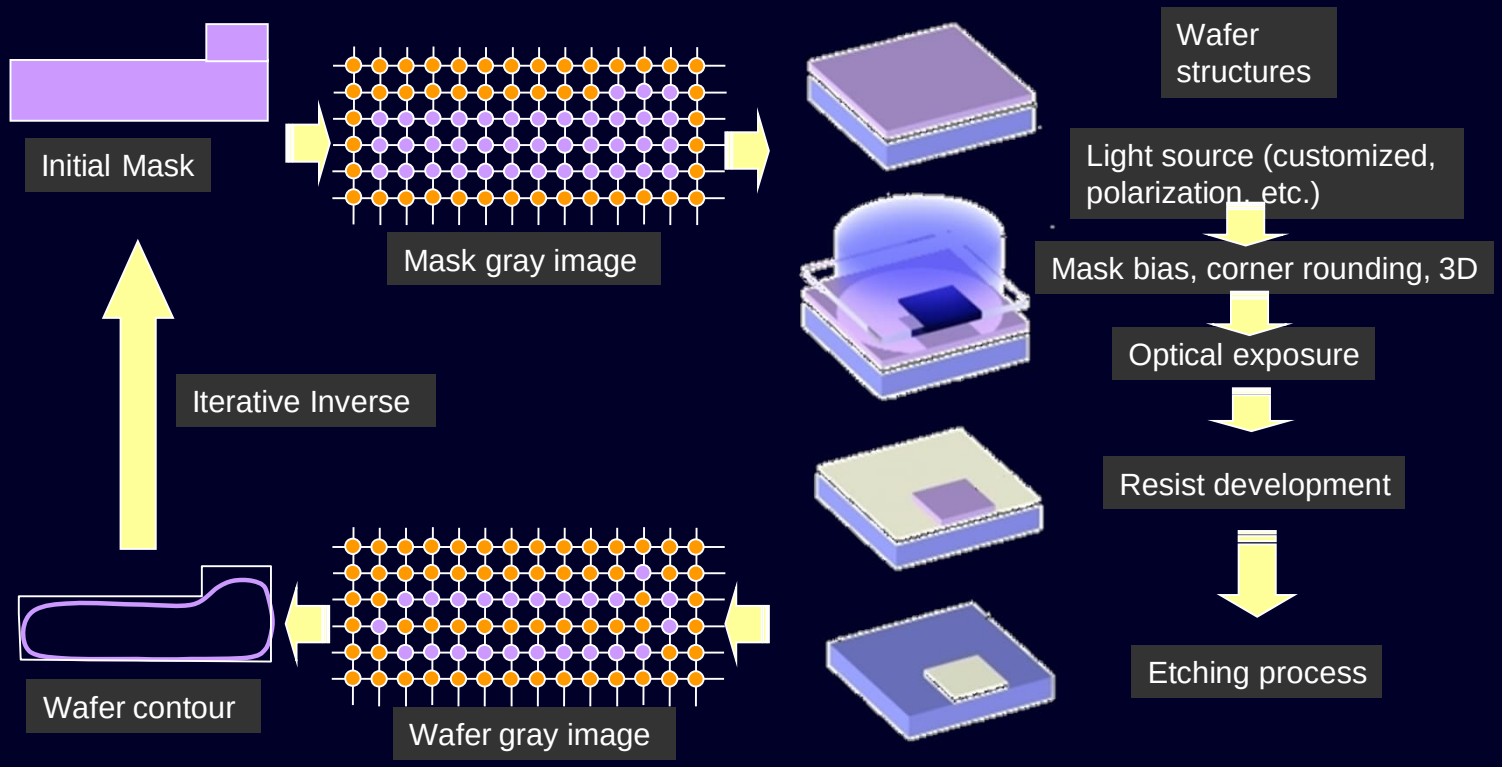
How ILT Works



ILT was first introduced by Luminescent as a viable alternative to OPC in 2005.

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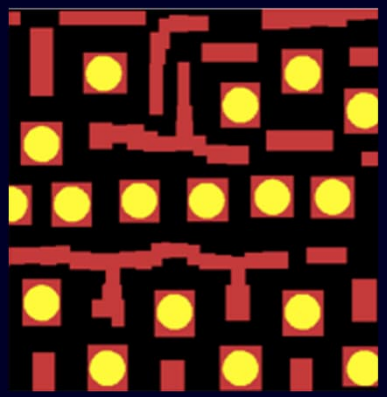
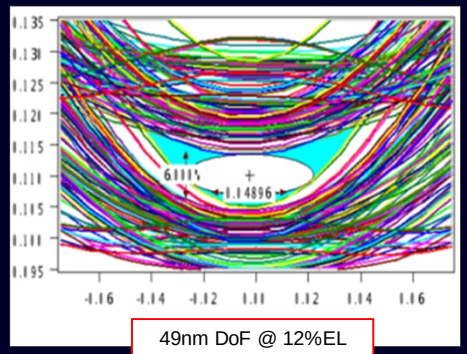
ILT Curvilinear Mask Delivers Superior Process Window

Manhattan OPC vs Curvilinear ILT

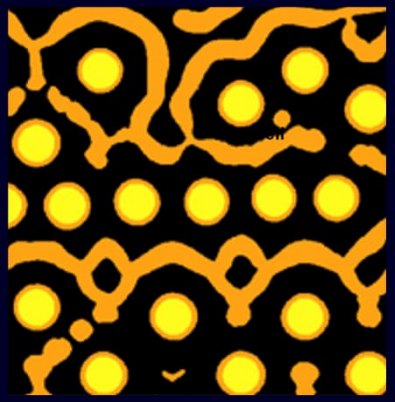
Standard OPC

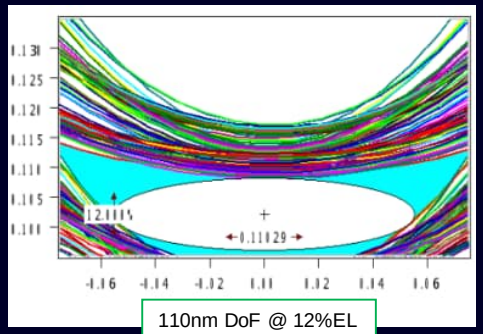




>2x increase in DoF

Curvilinear ILT





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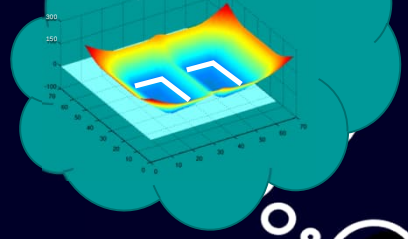
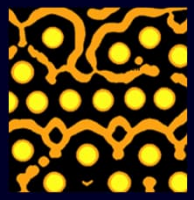
The Long Road to High Volume Manufacturing

2002 - 2003

Origins of ILT



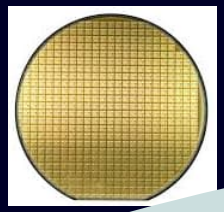
2004 - 2006



New Correction Technology

2007 - 2020

Industry Deployment Growing Pains



ILT High Volume Manufacturing

2021~

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ILT For HVM: An Odyssey

The first Adoption of ILT was by memory foundries

- Highly repetitive patterns lessen computation cost
- Careful crafts on a few repeating patterns are feasible

Achilles heels of ILT for Logic

- Long run time (~20x traditional OPC)
- Long mask write time (~10x Manhattan mask)
- MRC (what is the mask rule for curvilinear mask?)

Market Force

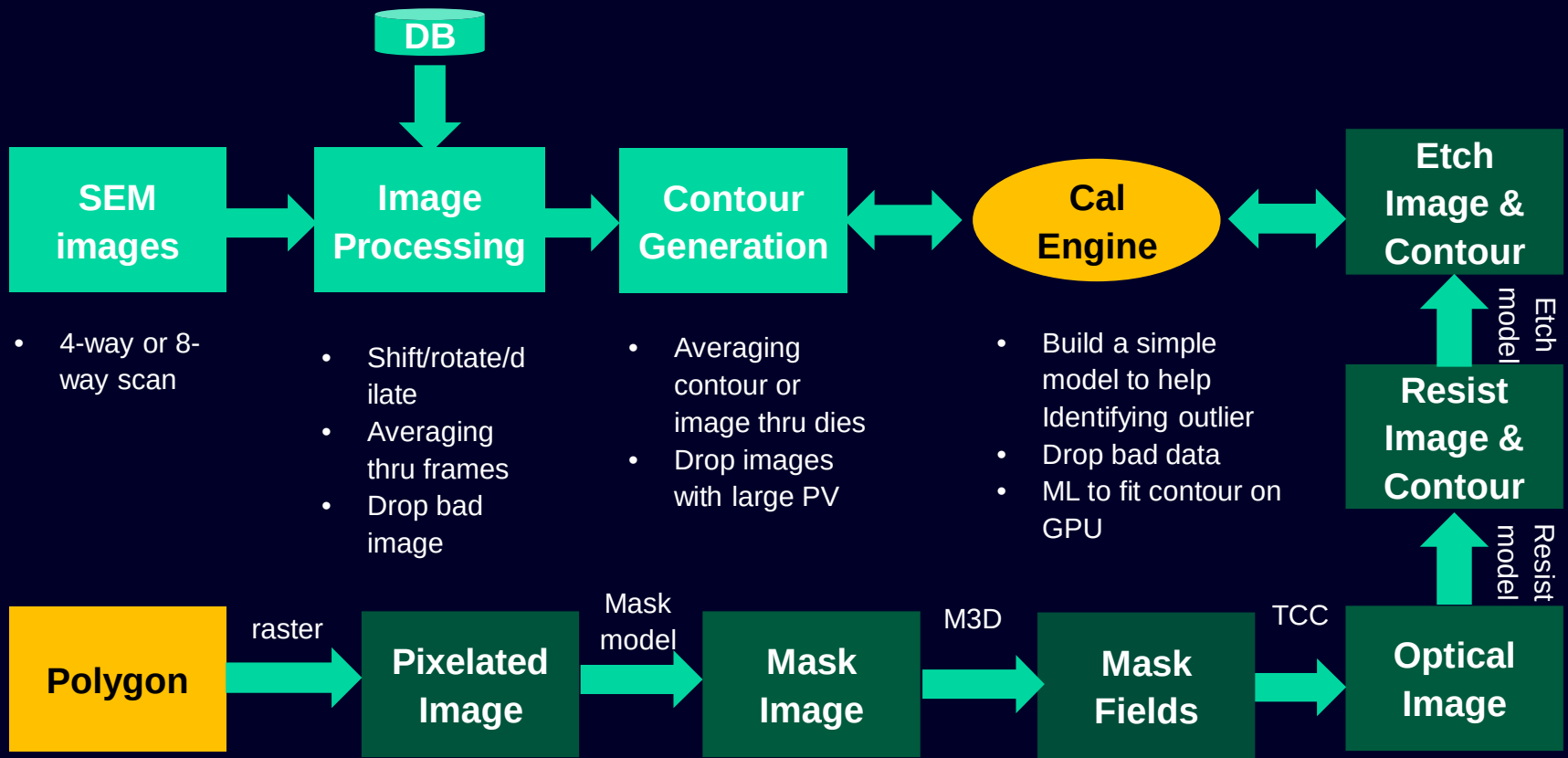
- The emerging of immersion lithography improves resolutions, making ILT not a must-have for the nodes at the time
- Better control of process variation (DOF@EL)

Nvidia Comes to the Rescue…

Sometime in late 2017, the author run into John Chen of Nvidia at a crowded restaurant in Royal Hsinchu hotel, and we started talking about the patterning challenges in making Nvidia GPU chips, and the author told him there was a solution, but it runs too slow, and he asked: why don't you use GPU to make my GPU? When he came back to San Jose, he introduced the author to two very dedicated NV engineers, Srinivas and Jerry. The rest is history.

John Chen of Nvidia former TSMC VP

GPU Requires a New Way of Model Simulation and Calibration



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ILT Speedup on Calibre

Operation	% of Total	Target GPU Speedup
Image Simulation	55.2%	10
Mask*	47.7%	10
SOCS	7.52%	50
CM1	19.4%	50
Objective Calculation	3.4%	10
Gradient Compute	7.5%	10
Projection	5.7%	10
Others/Misc.	28.2%	

**** Mask value reported includes everything not SOCS, under AI computation, including all geometry/rasterization***

Fast Forward To 2024……

Achilles Heels of ILT Healed:

- The rising of GPU can improve the ILT speed by >20x
- Multiple-Beam Mask Writer (MBMW) can write curvilinear mask (with moderate constraints) in constant time.
- ML can model mask-writing, lithography and etching process with un-precedent accuracy that enable astrom-level control to the location and dimension of printed pattern.

New mask format is getting ready to address the file sizes in transmission and storage

- SEMI Curvilinear Task Force sponsored by industry heavy-weight (TSMC, Intel, Samsung, IMS, NuFlare, Siemens EDA, ASML Brion, Synopsys…) convened to work on a file format.
- A standard Semi P49 is tentatively approved in March 2022, and formally approved in in March 2023.

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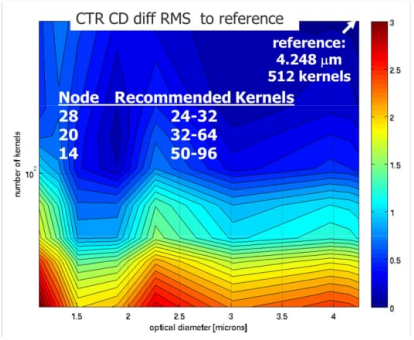
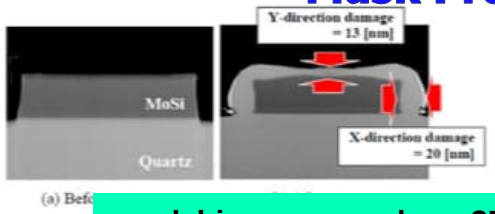
Holistic ML Model of Multiple Process Effects

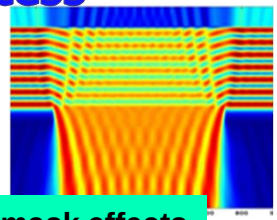
Scanner Optics

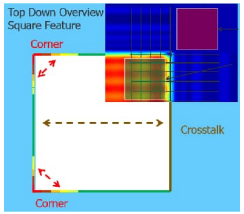
Lens aberrations Source representation



Mask Process

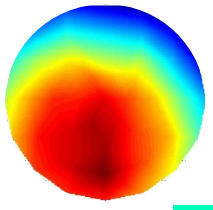


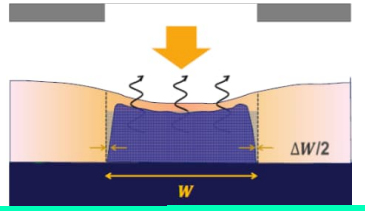


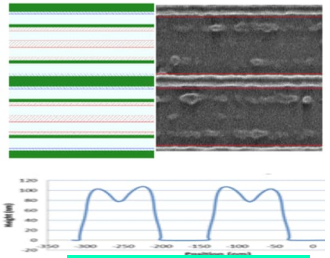


mask bias, corner chop, 3D mask effects

Resist Process





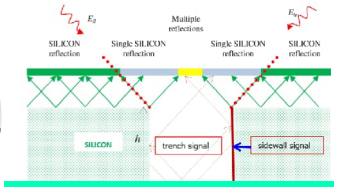


Pinch/Bridge NTD Resist

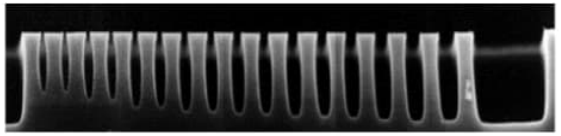
Resist Toploss

SRAF Printing

Etch Process



Implant topography



Etch Process

Micro-Loading

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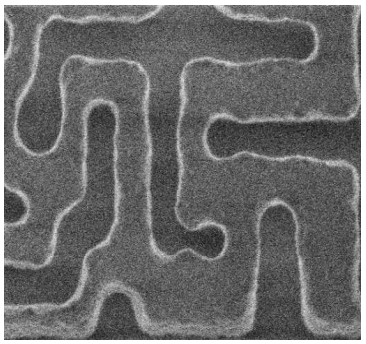
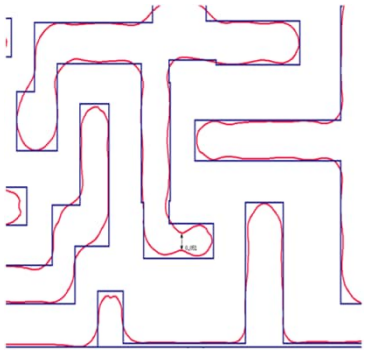
Contour-Based ML Model Calibration Can Predict the Location and Dimension

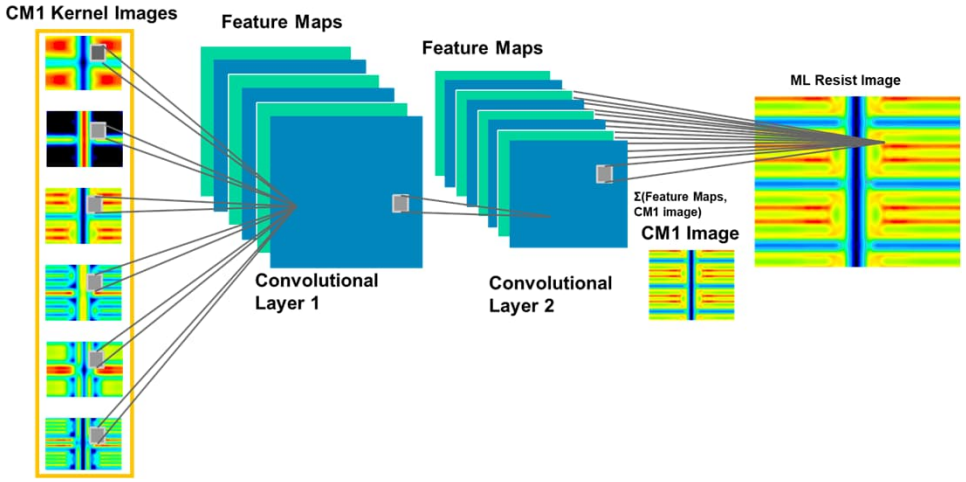
Wafer SEM



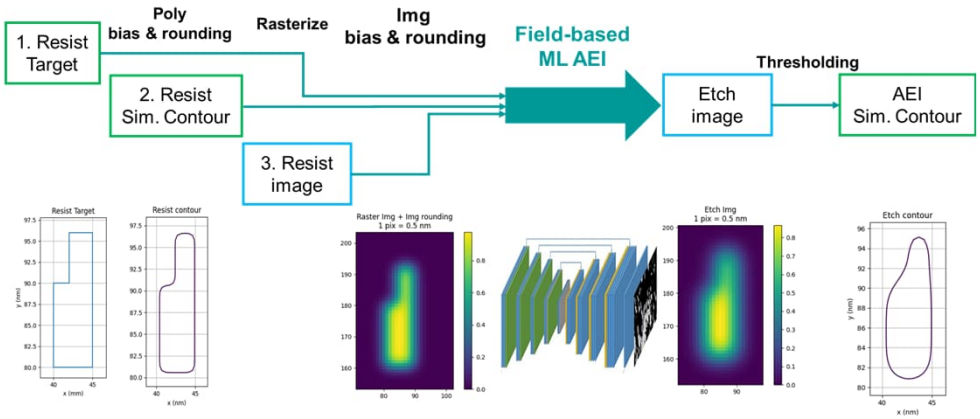
Contour extraction and alignment



CNN Based Resist



CNN Based Etch



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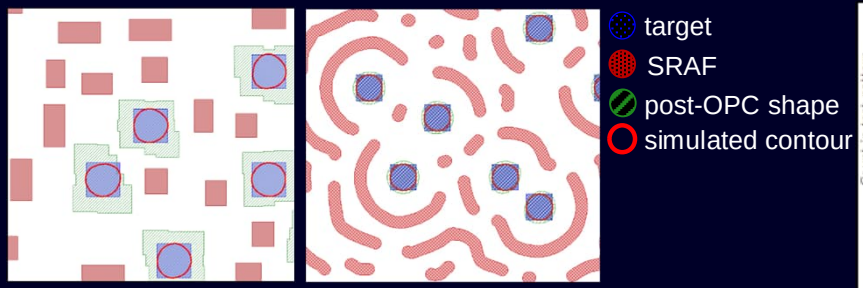
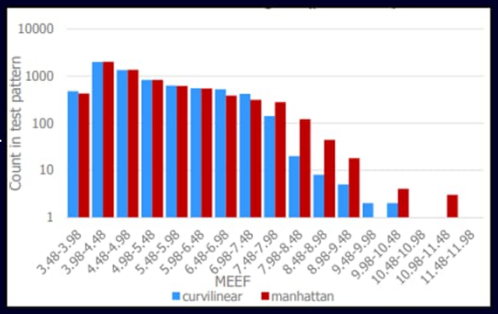
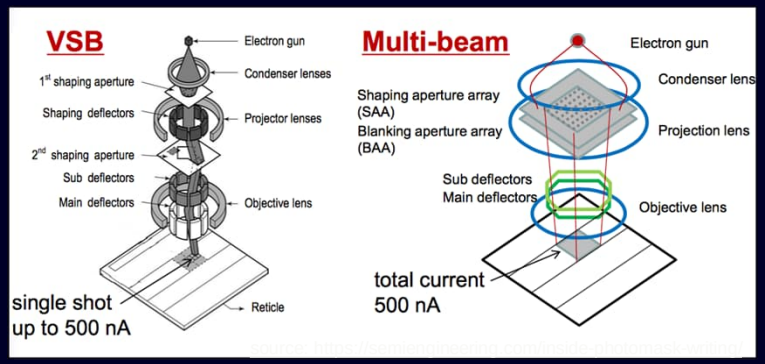
MBMW Can Write Curvilinear Mask IN Const. Time

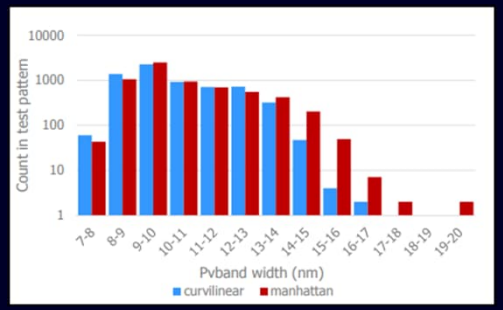
Traditional rectilinear OPC vs. CL SRAF and OPC







source: https://semiengineering.com/inside-photomask-writing/



The lithographic benefits were explored for curvilinear solutions.

The arrival of the multi-beam mask writers (MBMW) brings introduction of the CL masks to reality.

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Calibre Proivdes Complete Curvilinear End-to-End Solutions

Calibre SVRF

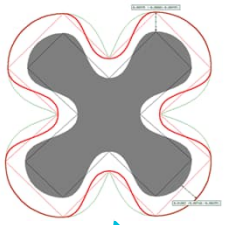
Calibre nmCLSRAF

Calibre nmCLOPC

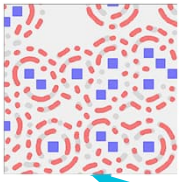
Calibre nmCLMPC

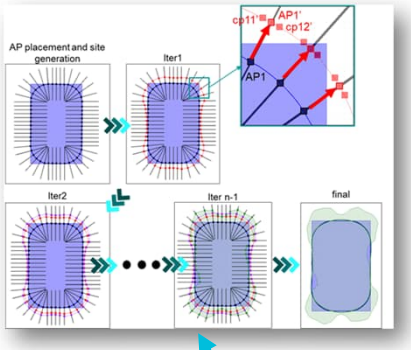
Calibre nmCLMRC

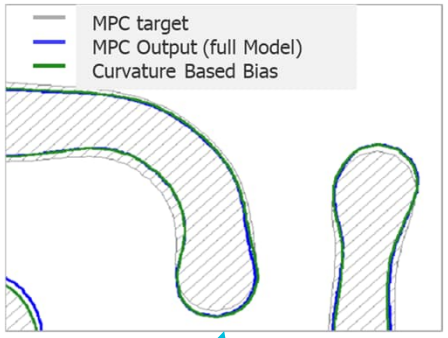
Calibre nmCLMDP

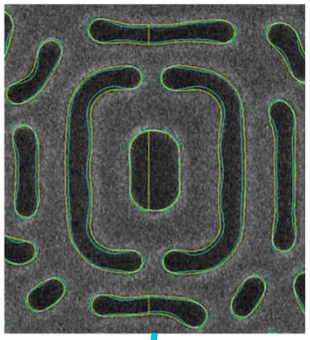


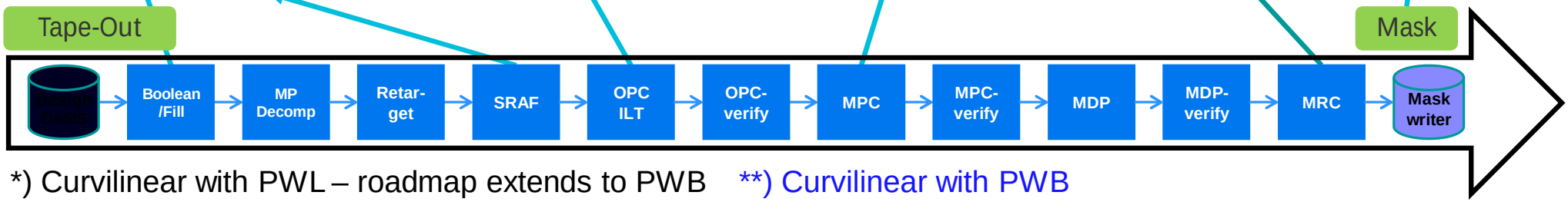
Calibre pxOPC











*) Curvilinear with PWL – roadmap extends to PWB **) Curvilinear with PWB

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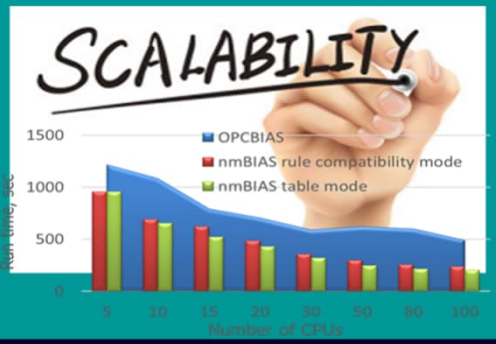
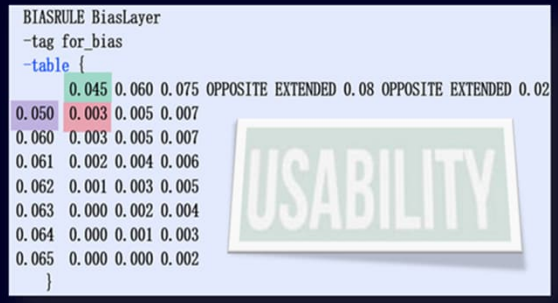
Quality and Accurate Rule-Based Curvilinear Biasing

- Spline-based biasing
- Smooth biasing results

Excellent Runtime Performance

- Scalable and efficient
- Meet runtime requirements





Easy-To-Use Biasing Table for Recipe Setup

- Great usability and flexibility
- User-defined customizable controls

Siemens EDA

Calibre nmCLBIAS

Calibre nmCLBIAS performs pre-OPC retargeting for curvilinear designs with enhanced capabilities that differentiate it from traditional pre-OPC retargeting tools.

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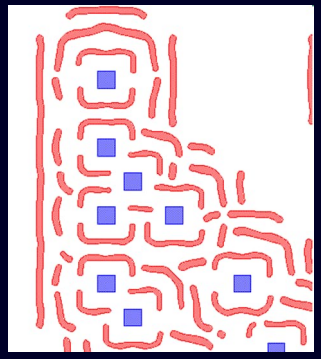
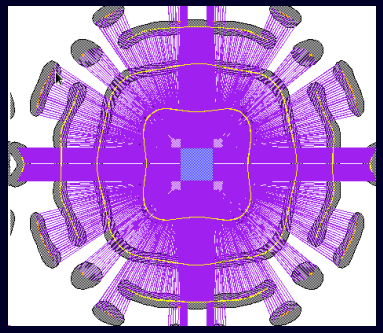


Fast and Accurate Rule-Based Curvilinear SRAF insertion

- Ray based rules for curvilinear SRAF insertion

Excellent Runtime Performance

- Fast rules-based solution
- ILT based templates



Automated ray based rule extraction from ILT SRAF result

- Great usability and flexibility
- User-defined customizable controls

Siemens EDA

Calibre nmCLSRAF

Calibre nmCLSRAF performs rules based curvilinear SRAF insertion based on ILT result

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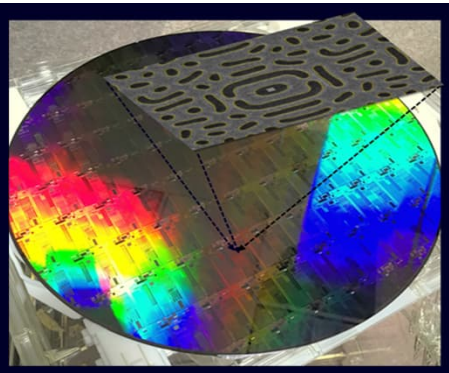
Siemens EDA

Calibre nmCLOPC

Calibre nmCLOPC performs model-based optical proximity correction for curvilinear edges to achieve high fidelity, smooth and consistent output that is mask-rule clean.

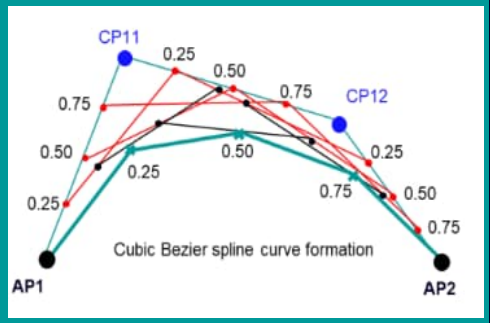


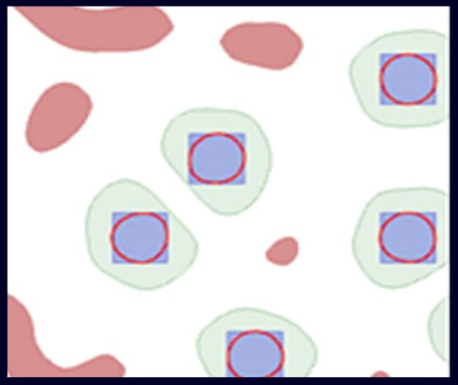
Fast Full-Chip Curvilinear OPC Solution

- Hybrid ILT CLOPC flow
- Faster runtime than a full ILT solution

Native Curvilinear Polygon Representation

- Native representation with Bezier splines
- File size reduction with more efficient edge representation





Advanced CLOPC Modeling

- Accurately model the mask 3D electromagnetic field effects for curvilinear masks
- Achieve the required accuracy

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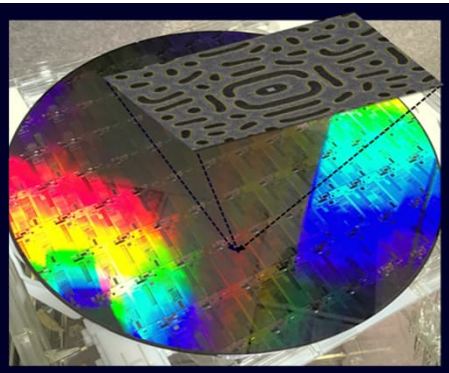
Siemens EDA

Calibre pxOPC

Calibre pxOPC performs model-based image optimization (SRAF & Main Feature co-optimization) for curvilinear mask technology. Various SRAF styles, Curvilinear MRC, extra print control, and integration with MEMOPC solutions are supported.

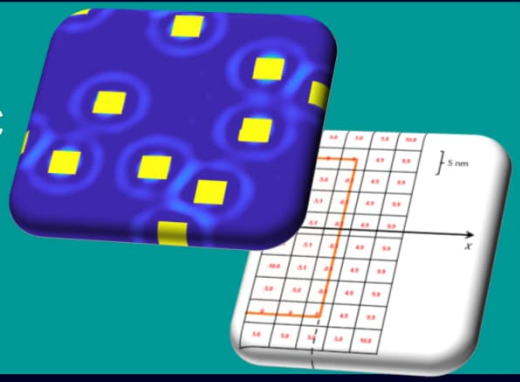


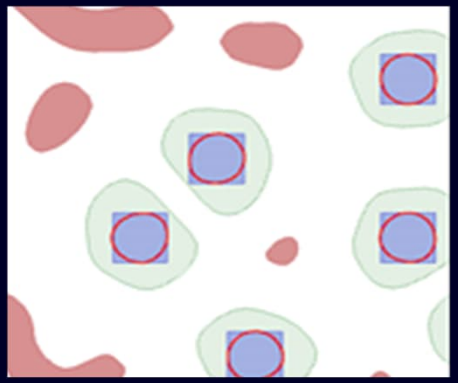
Accurate and Full-Featured Curvilinear ILT

- Integral part of Hybrid ILT CLOPC flow
- Integrates with MEMOPC for accelerated runtime

Native Curvilinear Polygon Representation at the core of pxOPC

- Multiple mask parameterizations supported internally for efficient representation during optimization





State-of-the-art mask correction

- High-NA EUV Stitching Compensation†
- Gradient descent optimization using custom in-house developed solvers – achieve aggressive correction for difficult cases

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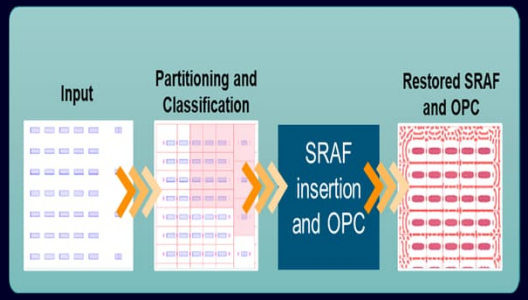
†*High-NA EUV Stitching currently under development; Anticipated release 2024.2*

Siemens EDA

Calibre RET MEMOPC

A replacement flow that ensures fast runtime and perfect consistency of correction across array, provides an extension across processing platform, as well as delivers integration work and refinement for symmetry and consistency.

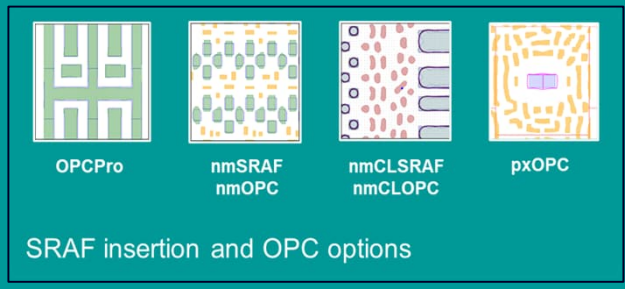


A Flow Infrastructure Solution

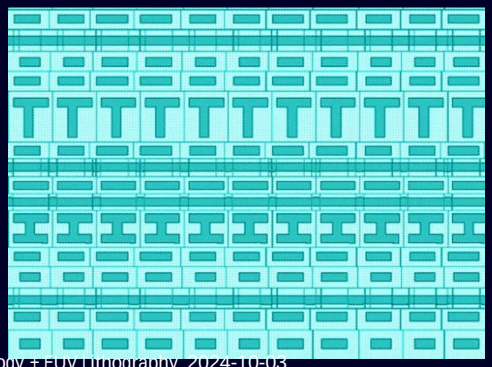
- A flow infrastructure solution with array/cell identification, SRAF/OPC insertion module, and array restoration.

Tool Selection Flexibility

- Various choices of OPC correction and SRAF Insertion.



SRAF insertion and OPC options



Meets the Requirement of Manufacturing Memory Devices

- Overcome the challenges of manufacturing memory devices and image sensor products which require processing approaches with geometric consistency and acceptable processing times.

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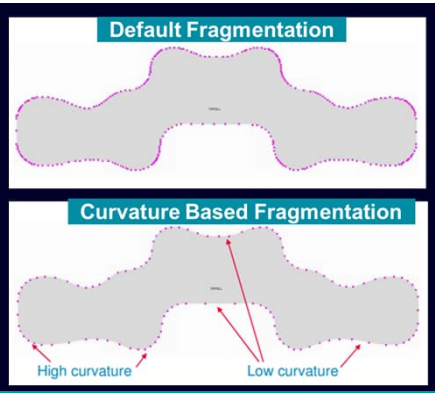
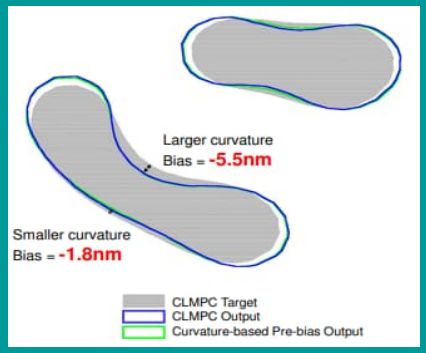


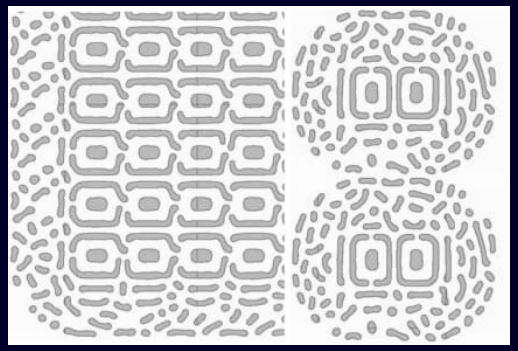
Innovative Curvature-Based Fragmentation

- Edge fragmentation based on local curvature
- Co-optimization with file size, accuracy, and execution time

Optional Curvature-Based Pre-Biasing For Faster Runtime

- Fast convergence for CLMPC without degrading the correction accuracy





Simultaneous Correction Capability

- MPC correction for curvilinear and rectangular shapes in one run

Siemens EDA

Calibre nmCLMPC

Calibre nmCLMPC supports curvilinear mask process correction to meet the expectations for processing time and mask pattern fidelity of advanced node curvilinear mask manufacturing.

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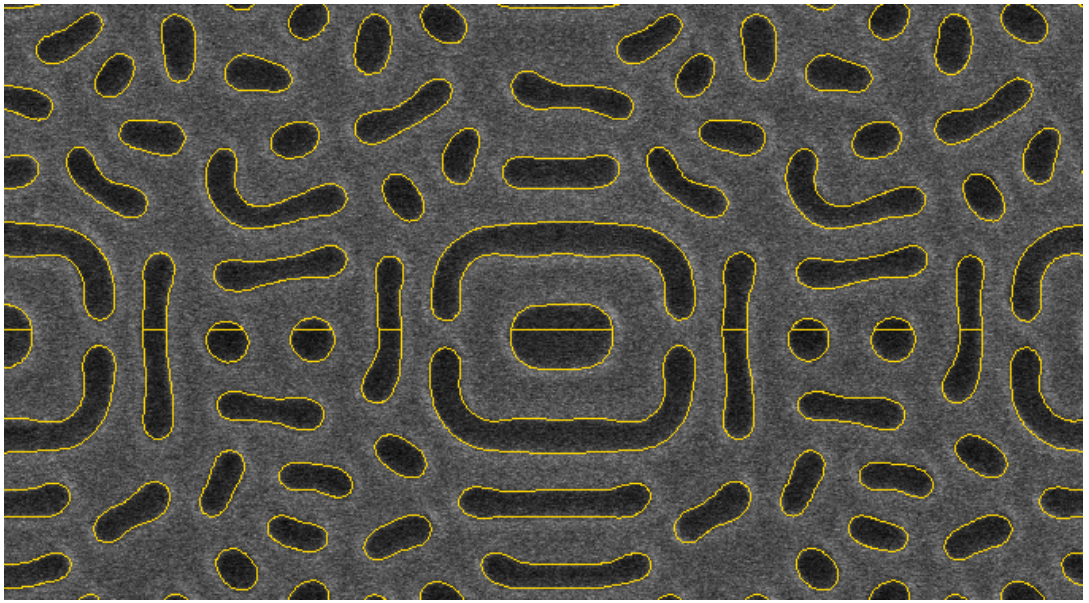
Post-MPC ILT patterns consistently print on target

- Curvilinear MPC enables printing complex mask shapes on target
- Accurate mask models and appropriate correction algorithms are key
- The entire tape-out flow from OPC to the mask writer will use the new multigon format to reduce data volume in correction engines and files



Target mask shape and simulated mask shape overlaid with post-MPC SEM image

Ingo Bork, et al., "Mask process correction validation for multi-beam mask lithography," Proc. SPIE 10810, Photomask Technology 2018; https://doi.org/10.1117/12.2503284

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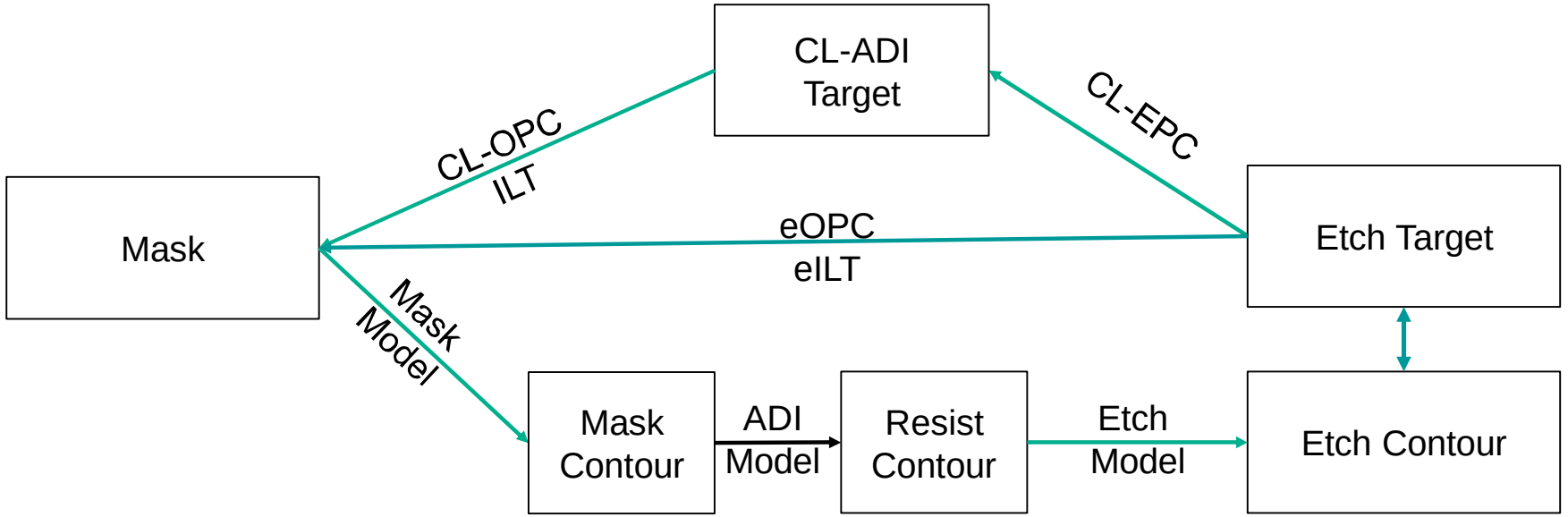
Mask Correction to Silicon---It Can Be Done Finally!



- One step model and correction
- Mask and Resist contour output for QC
- Make model learn profile information

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Future of Lithography Modeling and Mask Synthesis

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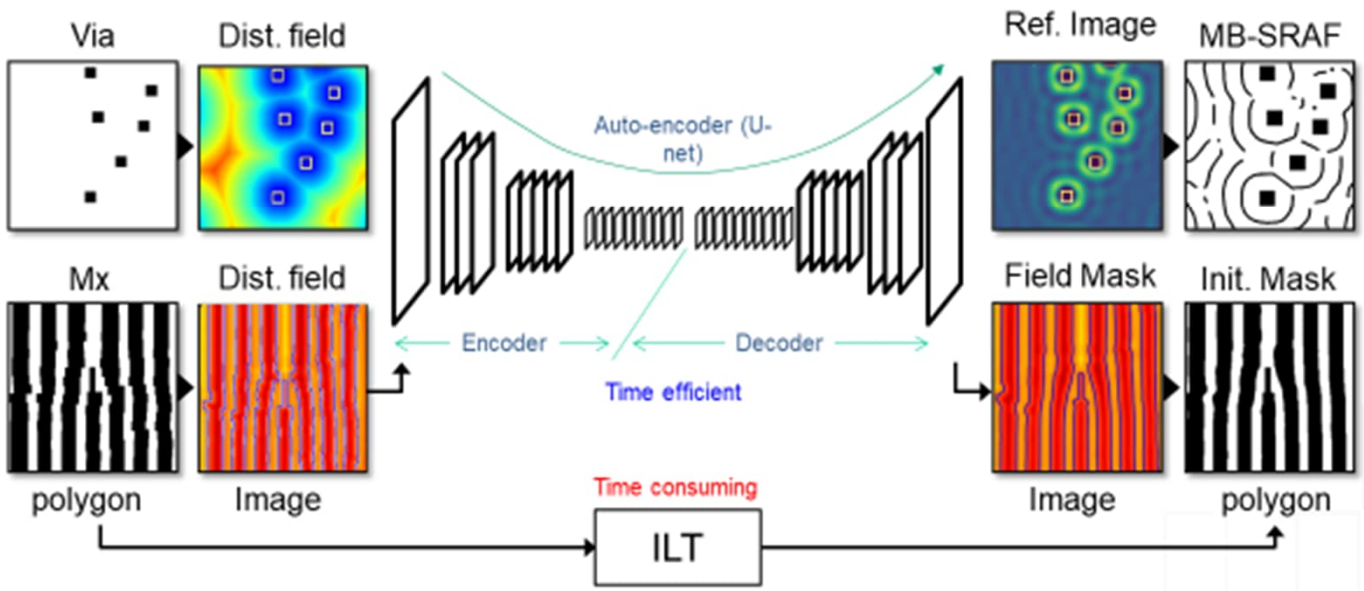
Deep Learning in Inverse Lithography Technology (ILT)



- DL aimed to reduce the TAT of mask corrections by pre-learning the corrected results.

	Layer 1	Layer 2
Applications	**SRAF seeding**	**Initial Mask**
Purpose	Model-based SRAF TAT reductions	ILT repair TAT reductions

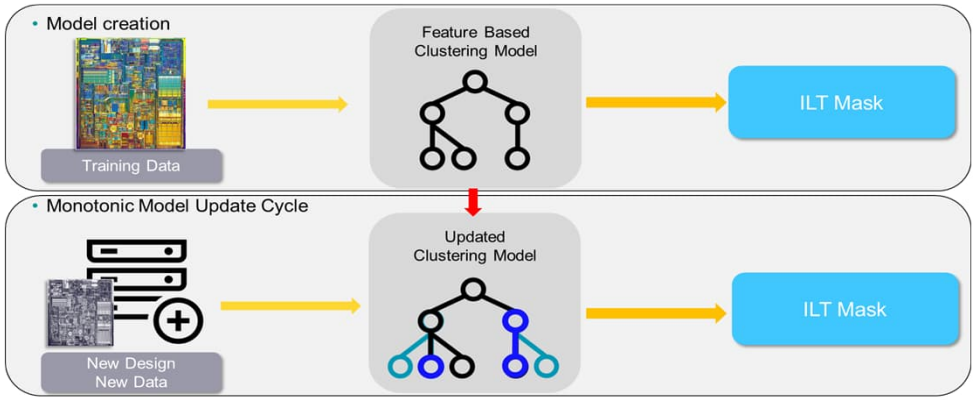
Source: Peng DAC 2021

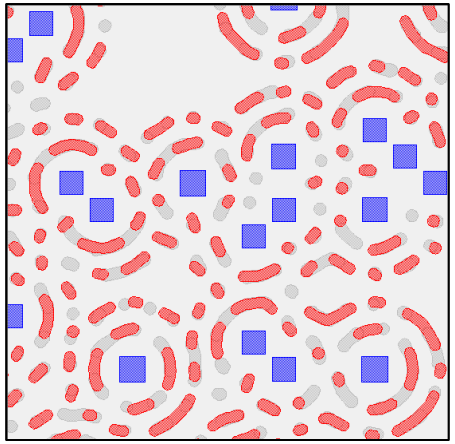
MML: ML ILT solution

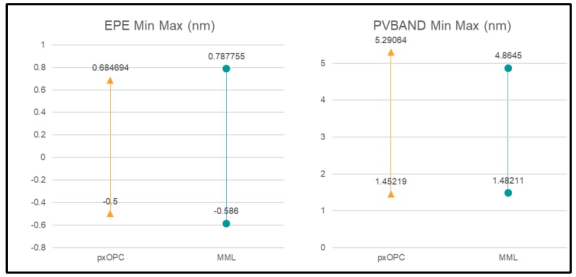
Monotonic Machine Learning (MML) is a machine learning mask synthesis solution for both *SRAF* and *Main Features*

- **Monotonic property of the model**
- For new design requiring model adjustments, the model appended *without changing unaffected clusters.*
  - Stable performance

Fast:
Performance of β-level ~*55x* faster than full-CLILT
SRAF prediction accuracy: F1 score > 80% on N2 logic layouts
Focusing on prediction accuracy, SRAF Cleanup, MRC compliance
MML can learn and predict any SRAF and main feature shape







MML SRAF
pxOPC SRAF

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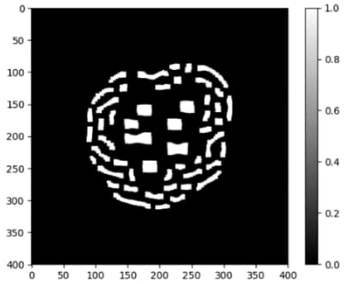
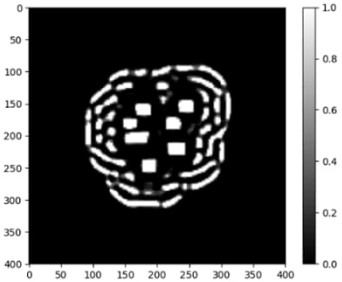
CNN for ILT

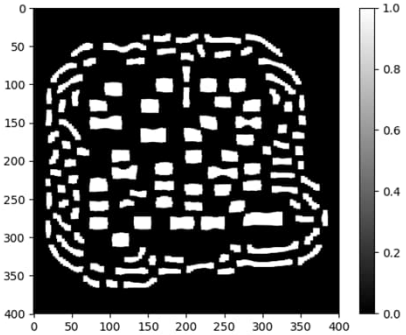
Baseline



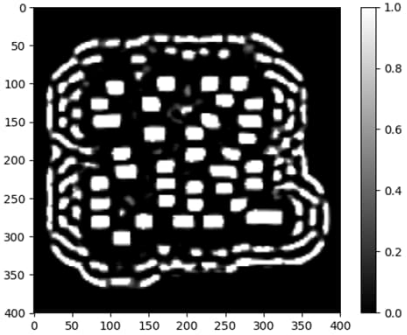
Predicted

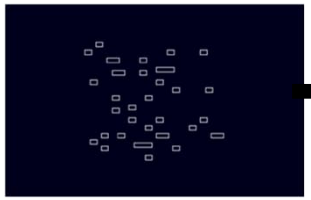


Baseline



Predicted

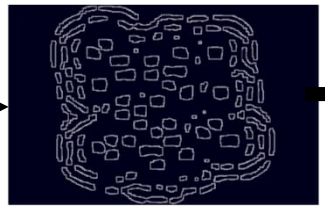




Raster

Generate Initial Mask

ILT cleanup



Repair

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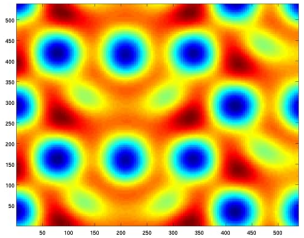
Resist 3D Modeling on GPU at Full-Chip Level

Aerial image from optics



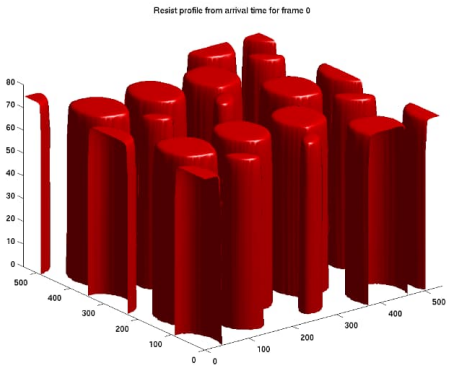
$$\begin{cases} \dfrac{\partial A}{\partial t} = \nabla(D_a \nabla A) - K_q A \cdot B - K_a A, \\ \dfrac{\partial B}{\partial t} = \nabla(D_b \nabla B) - K_q A \cdot B - K_b B, \\ \dfrac{\partial M}{\partial t} = -K_{amp} A \cdot M - K_m M. \end{cases}$$

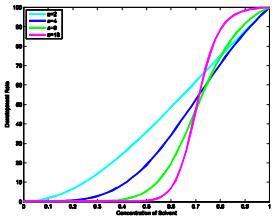
PEB: reaction-diffusion equations can be solved on GPU with orders-of-magnitude speedup

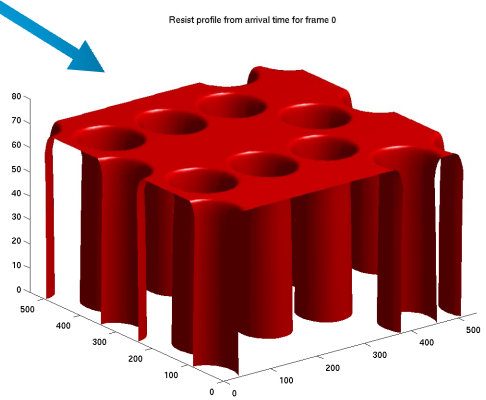
$$r(M)|\nabla T| = 1$$

Development: fast-sweeping method is orders of magnitude faster than front-tracking

PTD





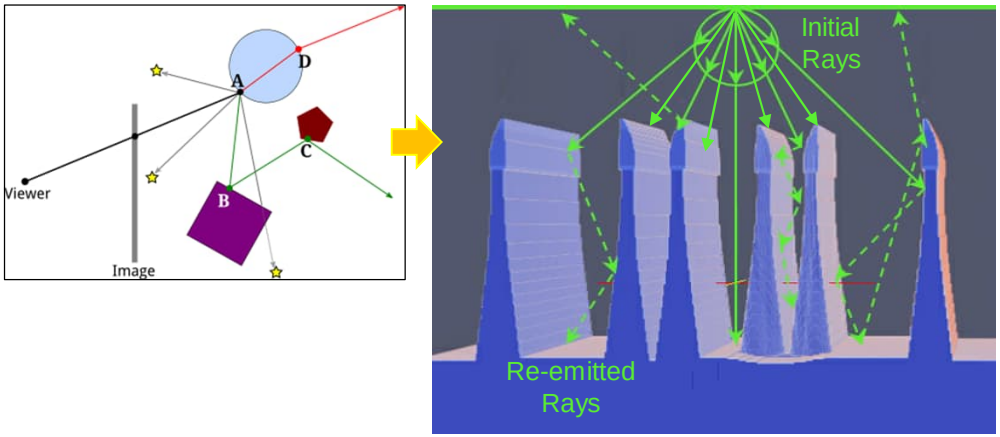


NTD

Etch Topo Simulation: Speed-up for Realistic Scale

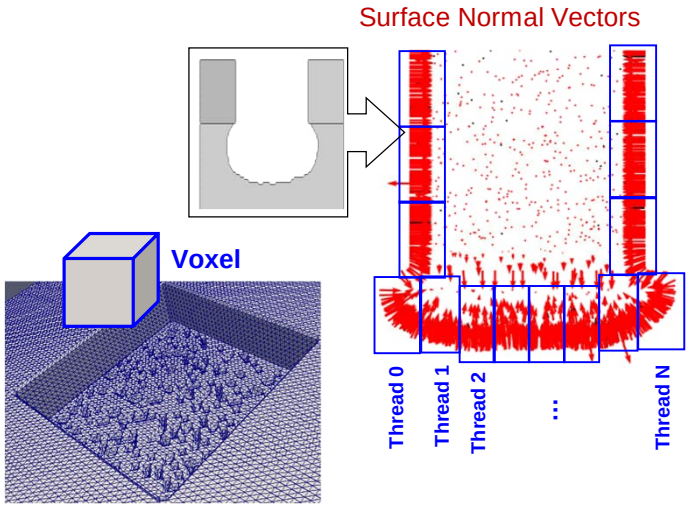
- HW-accelerated **ray-tracing algorithm** developed to calculate particle “hit points” on a surface.
- HW-accelerated **surface normal calculations** developed w/ spatial decompositions.

Ray-Tracing Implementation for Particle-Surface Collisions



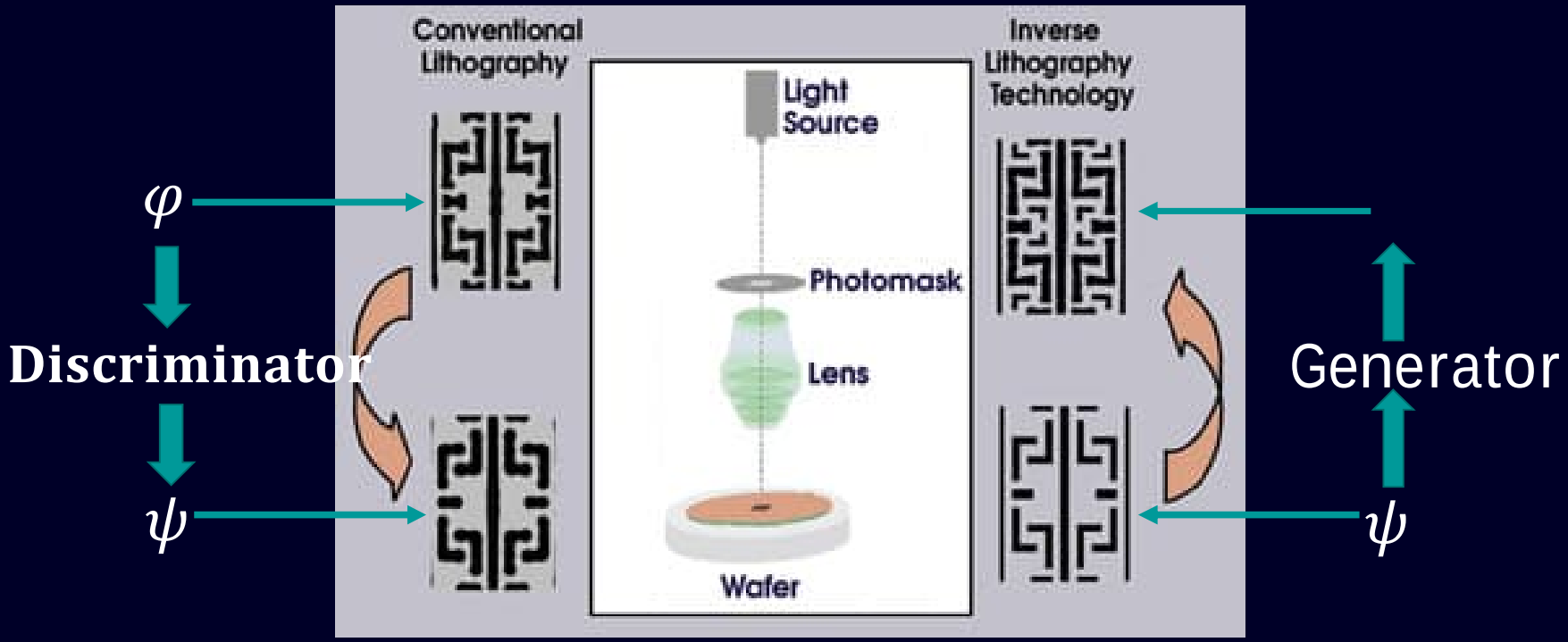
- Typical benchmark case:
  3D structure, 10^4 steps, 10^6 particles
  → 10^1~10^2 TAT reduction w/ 1 GPU card.

Parallelized Surface Normal Calculations



Voxel-based Mesh

Beating ILT with GenAI?



$$C = \sum_j c_j$$

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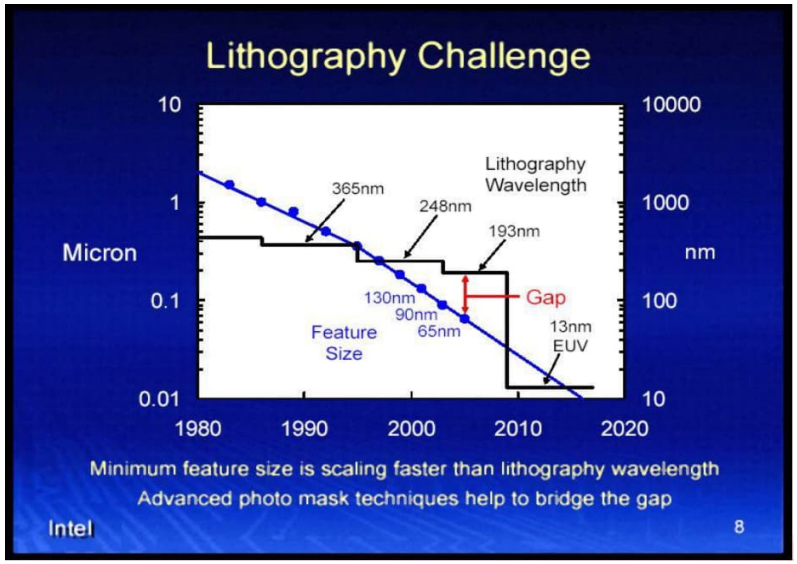
The Three Musketeers of Patterning Technology: Curvilinear, ML and GPU

Economic force:

- Relentless march of scaling

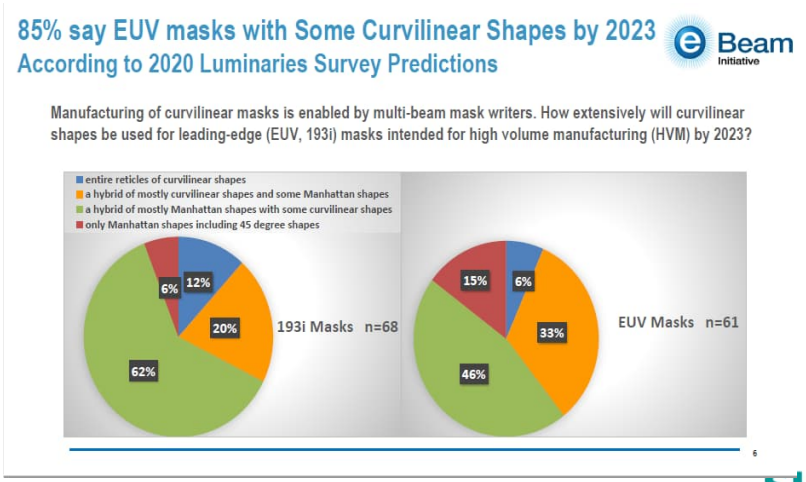


Market force:

- Scanner is getting very expensive
- Curvilinear mask can be used to squeeze more performance from the existing tool

Technological potentials:

- Emergence of curvilinear designs that are ideally suited for curvilinear ILT



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Unsung Heroes of ILT

Yuri Granik
Mentor Graphics

Luminescent

Peter Hu

Dongxue Chen

Tom Cecil

Guangming Xiao

Leo Pang

TSMC

Daniel Beylkin

Sagar Trivedi

Ken Ho

Jue-chin Yu

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Acknowledgements - The GPU and ML part of OPC simulation and ILT are developed with various CUDA libraries and with the great support from Nvidia engineering team. The author would like to thanks the contributions from the following individuals:

Srinivas Kodiyalam

Mark Kilgard

Levi Barnes

Max Katz