SIEMENS EDA

Shrinking the Die

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1.Objective

The current utilization ratio of the baseline database stands at 0.4 and the target is to achieve a ratio of 0.6 and address any physical pin violations. This support kit demonstrates three ways to achieve a higher utilization ratio, ultimately resulting in reducing the area of the die.

2. Introduction

Background: Die shrinkage via floorplan minimization is a process used in semiconductor design to make the chip smaller by carefully organizing its components without compromising its performance or functionality. This process starts of reduction in size of chip area starts with the first physical implementation stage, floorplan, by rearranging. the functional blocks—such as memory input/output (I/O) circuits, and logic gates—inside the chip's physical boundaries.

Utilization Ratio: (Area occupied by design components) / (Total available chip area)
Example of Utilization Ratio: For this design, present utilization ratio is 0.4, which draws attention to two important aspects of the design:

- **40%** of the die area is reserved for design **components** (standard cells).
- **60%** of the die area is reserved for the **routing** interconnects.

Need of Higher Utilization: Higher utilization ratio yields more effective space usage; dense packing of components results in smaller chip size while a lower utilization ratio indicates enough unused space that could potentially be utilized for additional functionalities.

Factors Influencing Utilization Ratio: The Utilization Ratio depends on how designers allocate space for physical components and routing resources, influenced by the design's size and complexity. Larger designs offer more flexibility, allowing for higher utilization ratios, while smaller designs may face stricter area constraints. A designer may target a utilization ratio of up to 0.8 (80% for components, 20% for routing) which is common, but careful planning and optimization are essential to avoid congestion and violations such as minimum area and pin overlapping. Therefore, choosing the utilization ratio requires careful consideration.

Conclusion: Thus, higher utilization would lead to higher integration densities, lower manufacturing costs, higher yields, and makes it easier to create smaller chip designs and, more effective integrated circuits.

3.Included Files

Demo data	A complete project and any necessary supporting files are in the db. directory. The project file is fp.proj.
Input file	A floorplan file which contains floorplan information named fp.tcl

4. Getting Started (Project set-up)

Step 1 Navigate to the floorplan directory and Invoke Aprisa session from the current working directory using command:

% AP

Step 2 Load the libraries imported project in the current AP session. Ensure the complete path for fp. proj. is included, i.e., the folder containing the floorplan project provided with this support kit.

% load_project <saved_directory_path>/db/fp.proj

```
  Top  Module : riscv_core
  Curr Module : riscv_core
{0403:16:18:14:LoadDsgn} Design   loaded: default/db/fp.proj (saved
r3:rhel7-64.2024.0204.1814 PST)
{0403:16:18:14:LoadProj} Project  loaded: default/db/fp.proj (saved
  2 21:36:27 2024)
```

Figure 1: A successfully loaded project.

The ***current project*** and ***loaded project*** will both be set when the project is loaded.

Step 3 Open the layout schematic by using command:

% open_layout

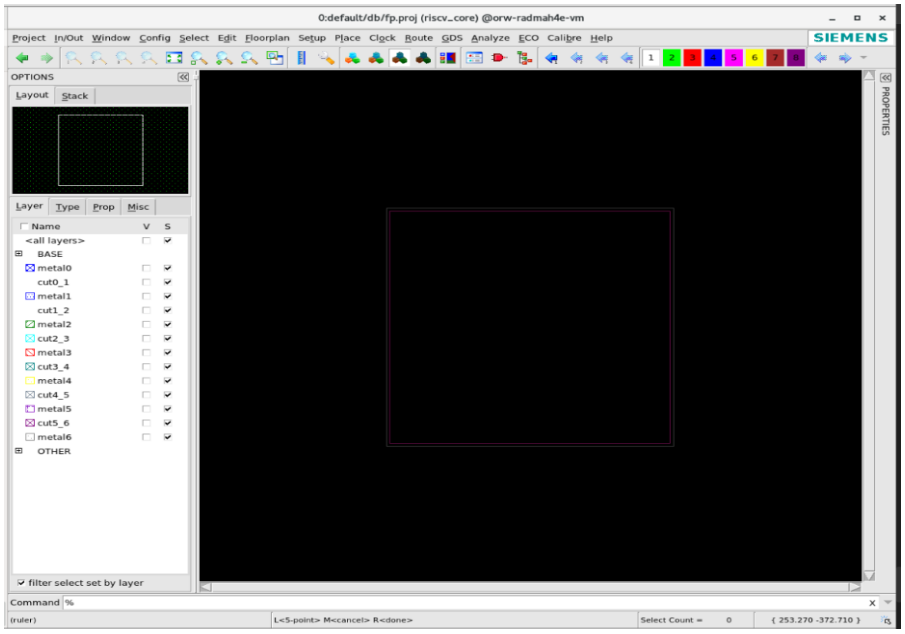

Figure 2: Layout window showing floorplan

5.Methods to Achieve Higher Utilization Ratio

Utilization Ratio can be increased using three ways:

1. By Ratio
2. By Size
3. By Co-ordinates

5.1. By Ratio

As discussed, utilization ratio is the measure of how efficiently the available chip area is utilized by the design components.

Utilization Ratio = (Area occupied by design components)/ (Total available chip area)

Another important factor to consider is, *Aspect ratio*, ratio of vertical to horizontal routing resources.

Aspect Ratio= (width of the design)/ (height of the design).

For the simplicity of this support kit, an aspect ratio of 1 is maintained, indicating equal height and width, resulting in a square-shaped design. The user may try different aspect ratio, such as 3.00, where the height is three times the width and observe how utilization ratio varies for different design shapes.

5.1.a. Objective

The objective of this section is to illustrate how to enhance the utilization ratio by increasing the ratio itself, using both APRISA GUI and TCL commands.

5.1.b. GUI Instructions

Step 1 To load the project, follow the steps mentioned in **Section 4. Getting started.**

Step 2 **Observe Original values:**

To begin, measure the utilization ratio, floorplan, physical pin locations of original design.

1. Report Utilization ratio:

Go to Aprisa shell, get the present utilization ratio details, using following command:

% ***report_placement***

```
----------
die utilization                 =  39.98 % ; C / X
core utilization                =  41.38 % ; (C - G) / A
std-cell utilization            =  41.38 % ; D / (A - F)
placeable-cell utilization      =  41.38 % ; H / B
```

Figure 3: Utilization 40% (Original)

2. Measure floorplan dimensions:

Go to APRISA layout window, zoom in to the layout to measure width and height of floorplan with the help of ruler using following steps:

- Press ***ctrl + R*** to open ruler window as shown below:

Figure 4: A ruler pop-up window

- Move the cursor to the layout window and place it at the top leftmost edge of the die. Drag the cursor to the top rightmost corner to measure the width of the die. Next, to measure the height, while keeping the mouse button pressed, move the cursor from the top rightmost edge to the bottom rightmost corner of the die boundary. Click the left mouse button twice to end the ruler. Close the ruler window. The measured floorplan values are shown in the layout below-

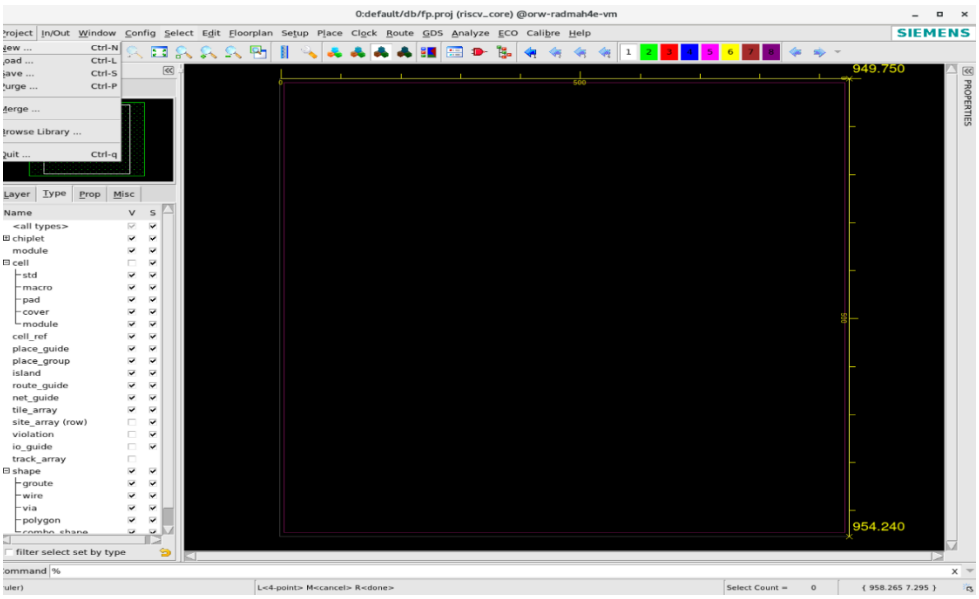

Figure 5: The measured height and width of original floorplan (Original)

Excerpt: To clear the ruler markers, press ctrl + R + shift from keyboard.

3. Physical pins location-

- Navigate to the APRISA layout window. On the left side, ensure to select the checkbox. labelled "<all layer>" to display pins on their respective metal layers.

.

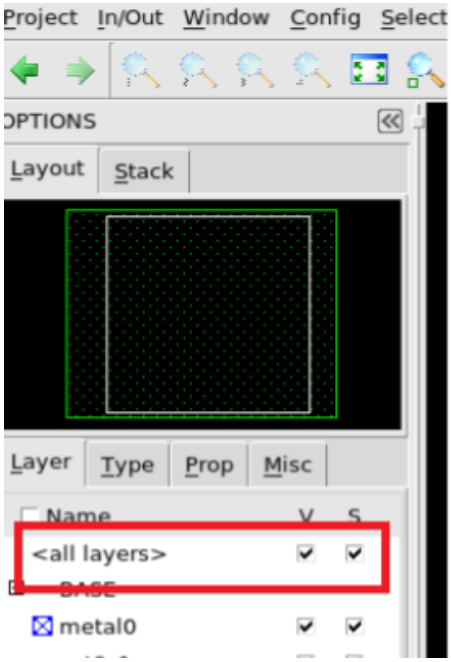

Figure 6: Layout window showing all metal layers are visible.

- To highlight the pin's location in the design layout, execute the following command:
  % select [get_phys_pins *]

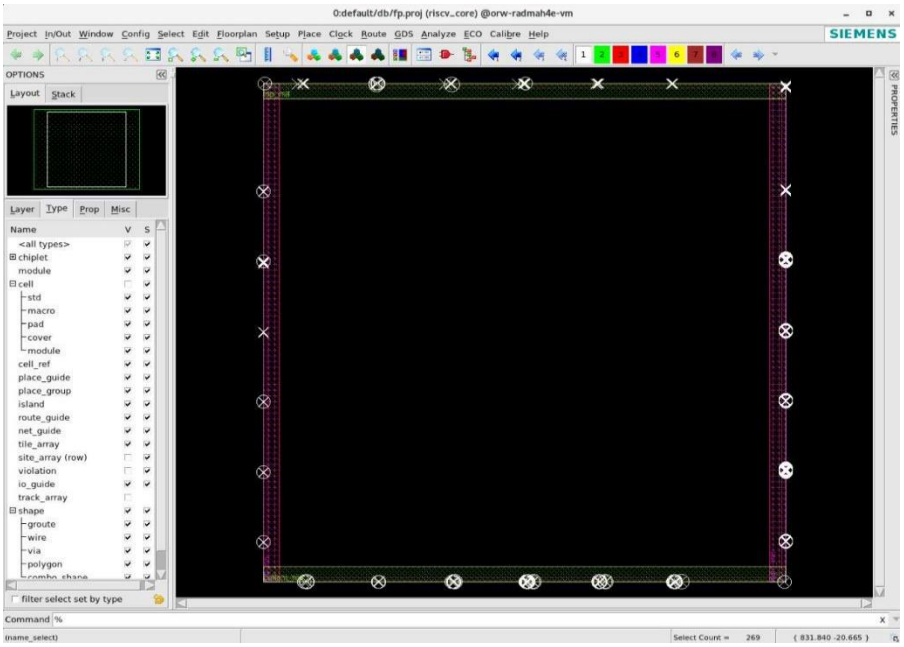

Figure 7: IO pins highlighted in the layout (Original location).

Step 3 Modify present utilization ratio**.** Select ***Floorplan*** from the Top Menu. This opens a sub-menu. Select ***Initialize Floorplan*** from the sub-menu to open the ***init_floorplan*** window.

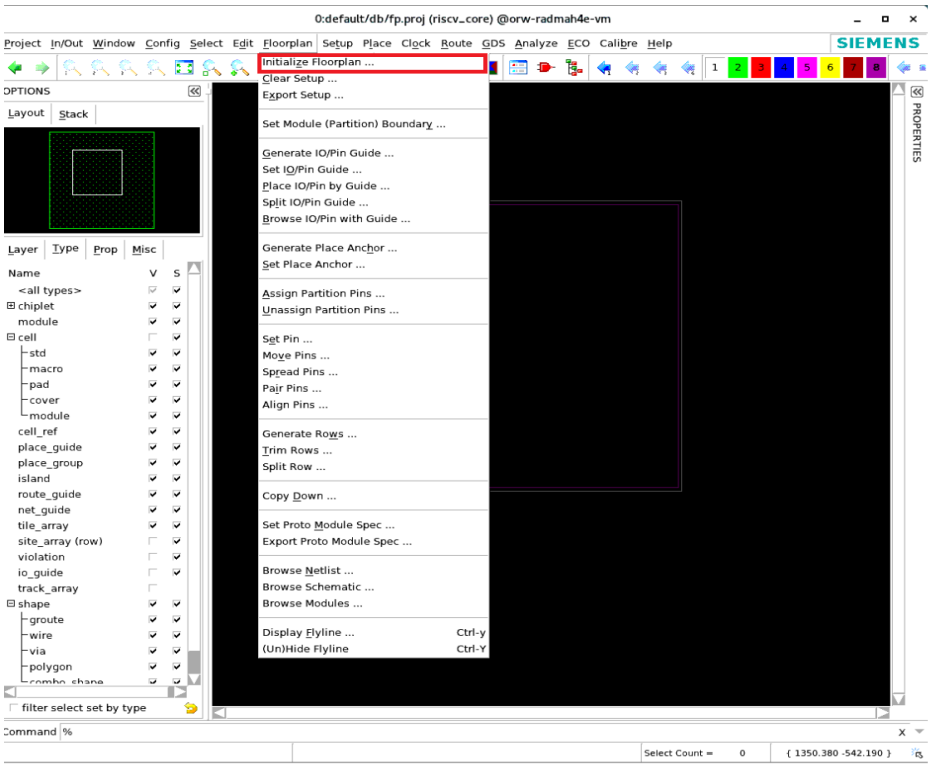

Figure 8: Floorplan options window.

Step 4 **Modify values:**

In the ***init_floorplan*** window, change the original values as mentioned below:

- Select Design Boundary: by_ratio.
- Keep Aspect ratio: 1.
- Modify current Utilization from 0.40 to 0.60

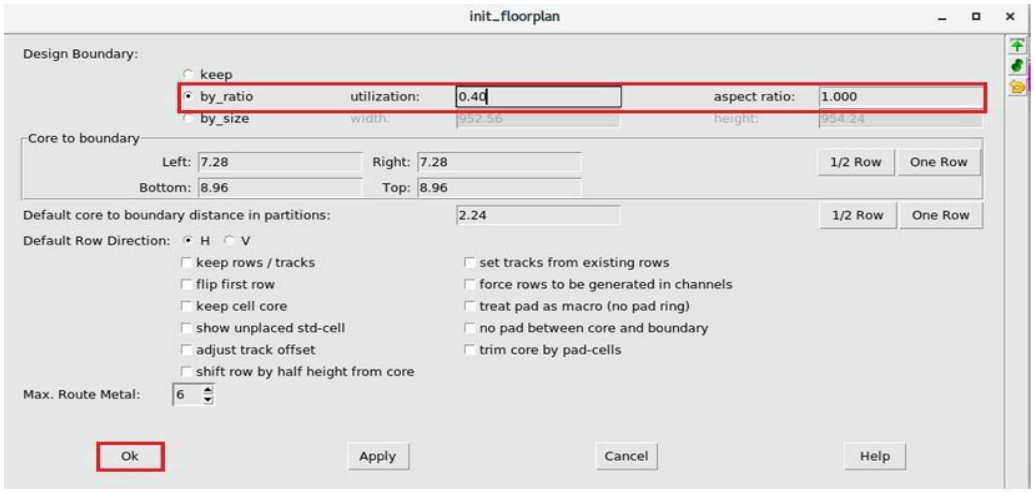

Figure 9: init_floorplan window with utilization ratio 0.40 (Original)

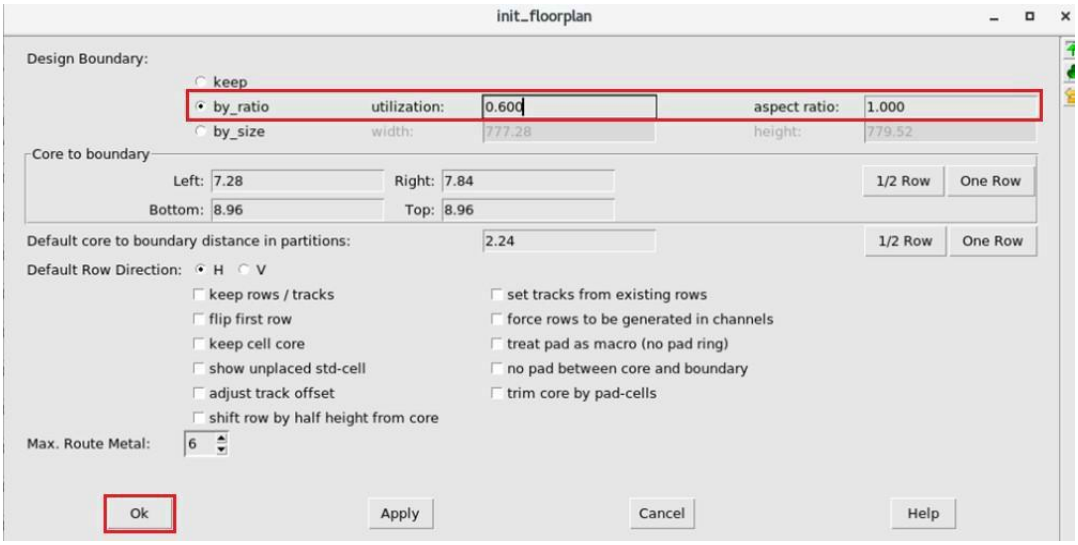

Figure 10: init_floorplan window with utilization 0.50 (New)

Step 5 Click ***Ok*** button and move back to Aprisa shell session.

Step 6

Modify physical pin's location:

Since the floorplan dimensions has changed, but the pins would yet remain at its original position, extending beyond the boundary and causing physical pin violations. This necessitates relocating. the existing physical pins according to the new design boundaries using following steps-

- Thus, check the current location of pins. To know how to verify pin's location,

Refer to **sub section 5.1.b** and go to **Step 2,** repeat **point number 3, Physical Pins Location.**

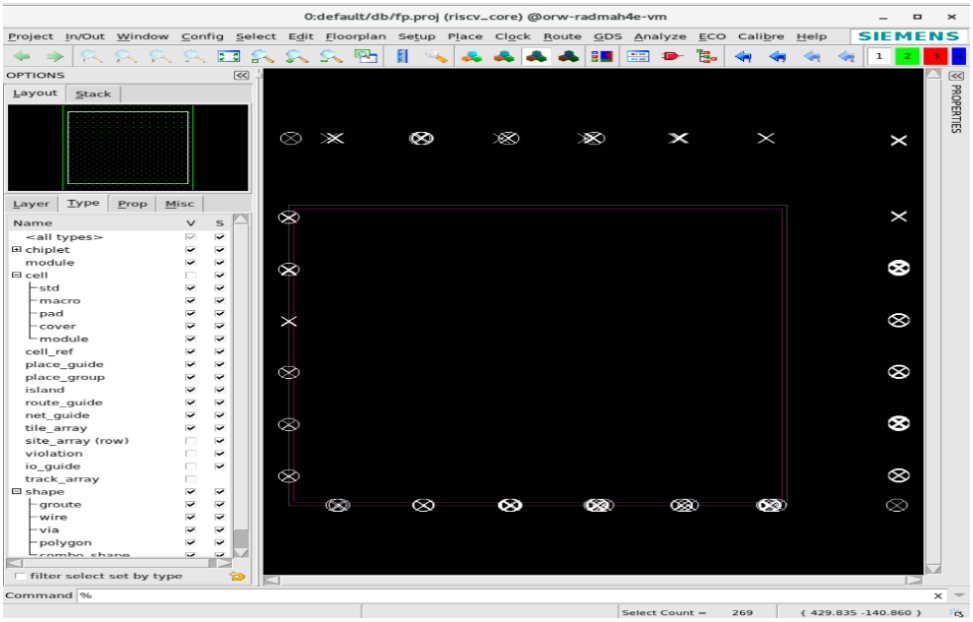

Figure 11: Highlighted IO pins outside of design boundary (Original pin location).

- Physical pin violations can also be get checked by using the following command:
  % ***verify_phys_pins***

```
Module has I/O-guide already, place I/O by guides
<0403:09:27:07:WARNING:LargeDftVia> Large default via: metal5 up   using 5 tracks : VIA56
<0403:09:27:07:WARNING:LargeDftVia> Large default via: metal5 up   using 5 tracks : VIA56
<0403:09:27:07:WARNING:CantUseNoPh> Lib cell has no physical info, treat as dont_use_in_opt: CLKVBUFJIHDLL
Floorplan initialized successfully
% verify_phys_pin                                    <0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation:
phys_pin_off_track - mem_d_resp_tag_i[0]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_track - mem_d_addr_o[3]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_track - cpu_id_i[7]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_track - reset_vector_i[26]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_track - reset_vector_i[21]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_track - reset_vector_i[15]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_track - cpu_id_i[20]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_track - cpu_id_i[16]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_track - cpu_id_i[9]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - cpu_id_i[24]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - mem_i_inst_i[15]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - reset_vector_i[5]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_overlap_block - reset_vector_i[4]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - reset_vector_i[4]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - reset_vector_i[3]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - reset_vector_i[2]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - cpu_id_i[31]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - cpu_id_i[30]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - cpu_id_i[29]
<0403:09:27:10:ERROR:PhysPinVio> phys_pin_violation: phys_pin_off_bndy_edge - cpu_id_i[28]
<0403:09:27:10:ERROR:PhysPinVio ... too many (> 20), print to log-file only ... >
169 phys_pin violations
```

Figure 12: Physical pin violations (189 total)

- Above, Figure 10, illustrates physical pin violations, totaling189. Thus, the current pin locations must be removed initially using the following command.

  % delete_object [get_phys_pins *]

```
% delete_object [get_phys_pins *]
delete phys_pin clk_i
delete phys_pin rst_i
delete phys_pin mem_d_data_rd_i[31]
delete phys_pin mem_d_data_rd_i[30]
delete phys_pin mem_d_data_rd_i[29]
delete phys_pin mem_d_data_rd_i[28]
delete phys_pin mem_d_data_rd_i[27]
delete phys_pin mem_d_data_rd_i[26]
delete phys_pin mem_d_data_rd_i[25]
delete phys_pin mem_d_data_rd_i[24]
+ ... 259 more
```

Figure 13: Deleted physical pins (old location)

- The new IO pins will be positioned on IO guides. Confirm the placement of existing. IO guides,
  using the following command

  % get_io_guides *

```
% get_io_guides *
{bottom_m2} {bottom_m4} {bottom_m6} {right_m1} {right_m3} {right_m5} {top_m2} {top_m4} {top_m6} {left_m1} {left_m3}
{left_m5}
```

Figure 14: Existing IO guides.

The naming convention provided by Aprisa would be as follows {<edge>_<metal layer_number>}

- Initial global IO placement of the pins can be done by using following command:

  %place_io -global_opt

```
% place_io -global_opt
ClockCellSpacing = 0
2 PG nets have shapes
m0 promotion: 0 (7, 1)
m1 promotion: 0 (0, 1)
m2 promotion: 0 (7, 1)
  puMgrInit           0 (1) Report
 TOTAL_CUT: X = 3206 Y = 2888
{0403:09:30:28:Place_io Finish     }        Elapsed = 00:00:00; CPU = 00:00:00; VM
Process-RSS =  349.4M (20.0%), System-Free = 151683.7M
```

Figure 15: Global IO pin placement.

- After the Global IO placement is executed, IO pins must be spread and positioned across IO slots using the following command.

  % place_io -by_guide

- After successfully placing the physical pins according to the new floorplan dimension, verify if there any violation left.

  % verify_phys_pins

```
% verify_phys_pin
0 phys_pin violations
1
```

Figure 16: Zero pin violation

Step 7 Observe New values:

Lastly, measure the utilization ratio, floorplan, physical pin locations of original design.

1. Utilization ratio:

Go to Aprisa shell, use following command to get the present utilization ratio details-

% ***report_placement***

```
utilization
-----------
  die utilization                  =  59.98 % ; C / X
  core utilization                 =  62.61 % ; (C - G) / A
  std-cell utilization             =  62.61 % ; D / (A - F)
  placeable-cell utilization       =  62.61 % ; H / B
```

Figure 17: Utilization 60% (New)

2. Measure floorplan dimensions:

Go to APRISA layout window and zoom in to the layout to measure width and height of floorplan using ruler. To know how to use ruler, refer to **sub section 5.1.b** and go to **Step 2,** repeat **point number 2. Measure floorplan dimensions.**

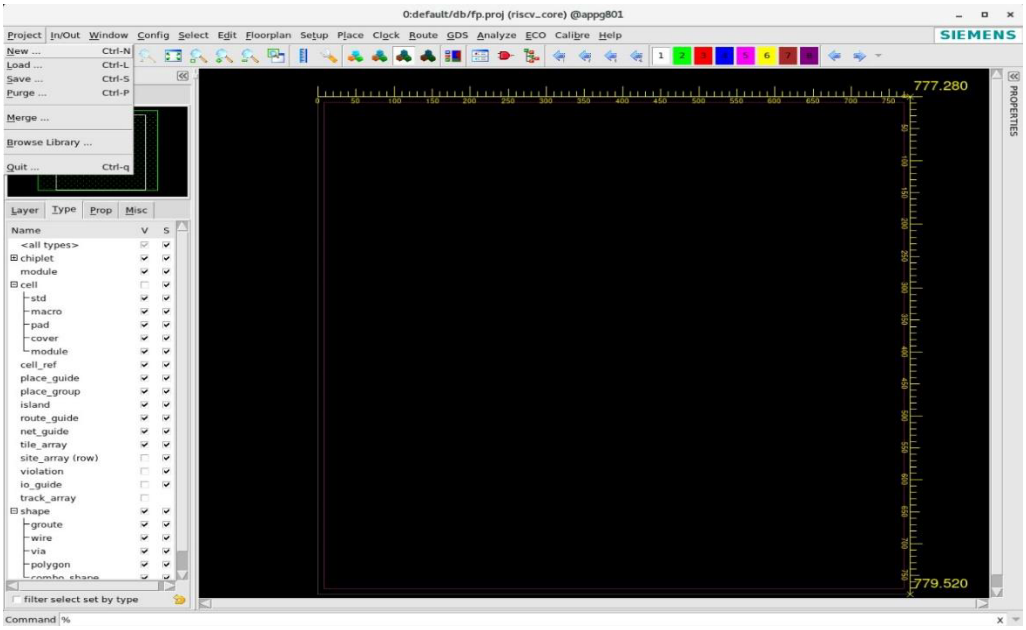

Figure 18: Measurement of height and width of original floorplan (New)

3.Verify the new location of physical pins-

Check the location of physical pins. To know how to verify pin's location, Refer to, **sub section 5.1.b**, go to **Step 2**, repeat **point number 3, Physical Pins Location**

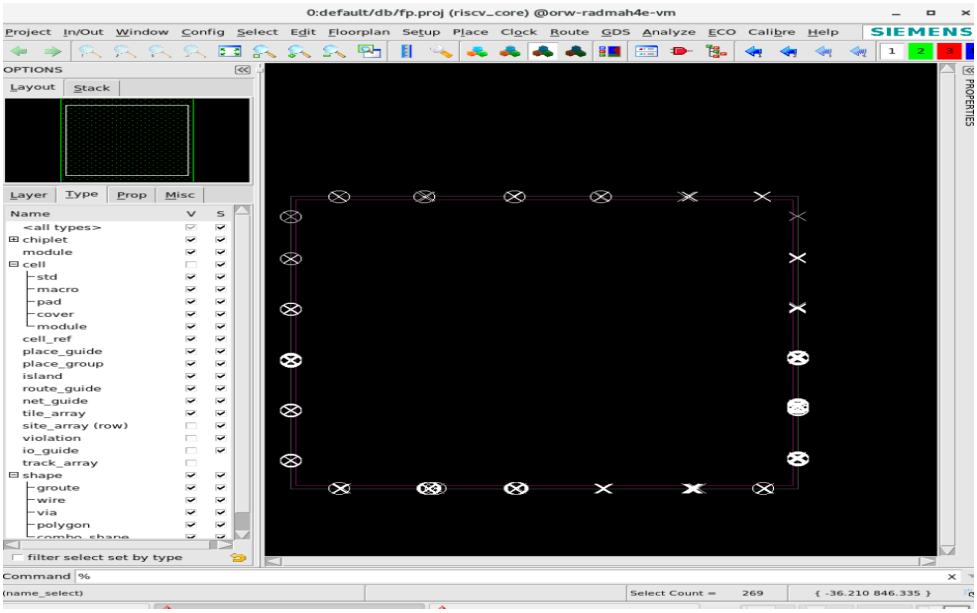

Figure 19: Highlighted IO pins inside the design boundary (New pin location)

Step 8 Exit the current session using the below command:

% exit

5.1.c. TCL Commands

Run the commands either in Command Line Interface (CLI) or Aprisa shell and see the changes in the layout window.

1.Load the project in Shell- % ***load_project default/db/fp.proj***

2. Change the utilization ration of floorplan by executing following command:
%init_floorplan -boundary by_ratio -utilization 0.45 -aspect_ratio 1.0 - max_route_metal 6 --keep_cell_core

3. To move physical pin location, Go to **Section 5.1. b**, repeat **Step 6.**

4. Observe the changes in the layout window.

5.1.d. Conclusion

In this exercise, it has been demonstrated, how to directly increase utilization ratio, using both the GUI and the TCL Command Line Interface (CLI) during the floorplan stage to ultimately reduce the die size.

Comparison between original and modified floorplan dimensions is shown below:

Utilization Ratio	Height	Width
0.4 (Original)	954.240	949.750
0.6 (New)	779.520	777.260

Excerpt: Use any other values of the utilization ratio in ***init_floorplan*** window, observe how floorplan changes its reduced in size.

5.2. By size

Height and width of the design.

5.2.a. Objective

The objective of this section is to illustrate how to enhance the utilization ratio at the floorplan stage by modifying the height and width of the design using both APRISA GUI and TCL commands.

5.2.b. GUI Instructions

Step 1 To load the project, follow the steps mentioned in **Section 4. Getting started.**

Step 2 **Observe Original values:**

To begin, measure the utilization ratio, floorplan, physical pin locations of original design.

1. Report Utilization ratio:

Go to Aprisa shell, get the present utilization ratio details, using following command:

% ***report_placement***

```
----------
die utilization                 =  39.98 % ; C / X
core utilization                =  41.38 % ; (C - G) / A
std-cell utilization            =  41.38 % ; D / (A - F)
placeable-cell utilization      =  41.38 % ; H / B
```

Figure 20: Utilization 40% (Original)

2.Measure floorplan dimensions:

Go to APRISA layout window and zoom in to the layout to measure width and height of floorplan using ruler. To know how to use ruler, refer to **sub section 5.1.b,** go to **Step 2,** repeat **point number 2.**

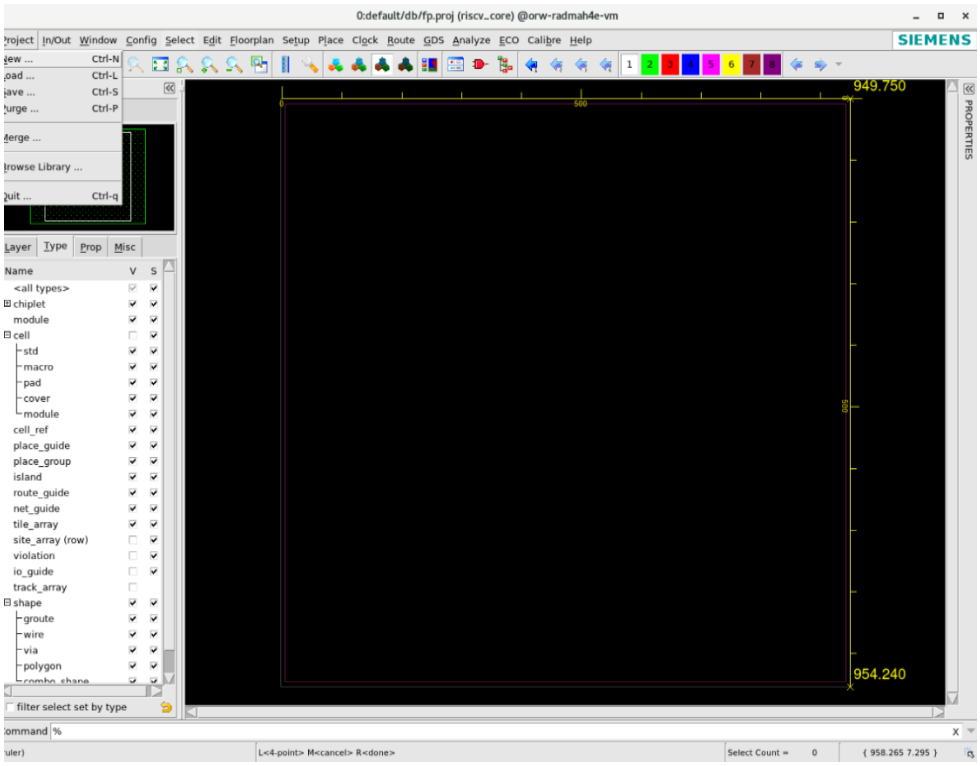

Figure 21: Measured height and width of original floorplan

3.Physical pins location-

Locate the original position of pins. To know how to see the physical pin's location, refer to **sub section 5.1.b,** go to **Step 2,** repeat **point number 3. Physical pin's location.**

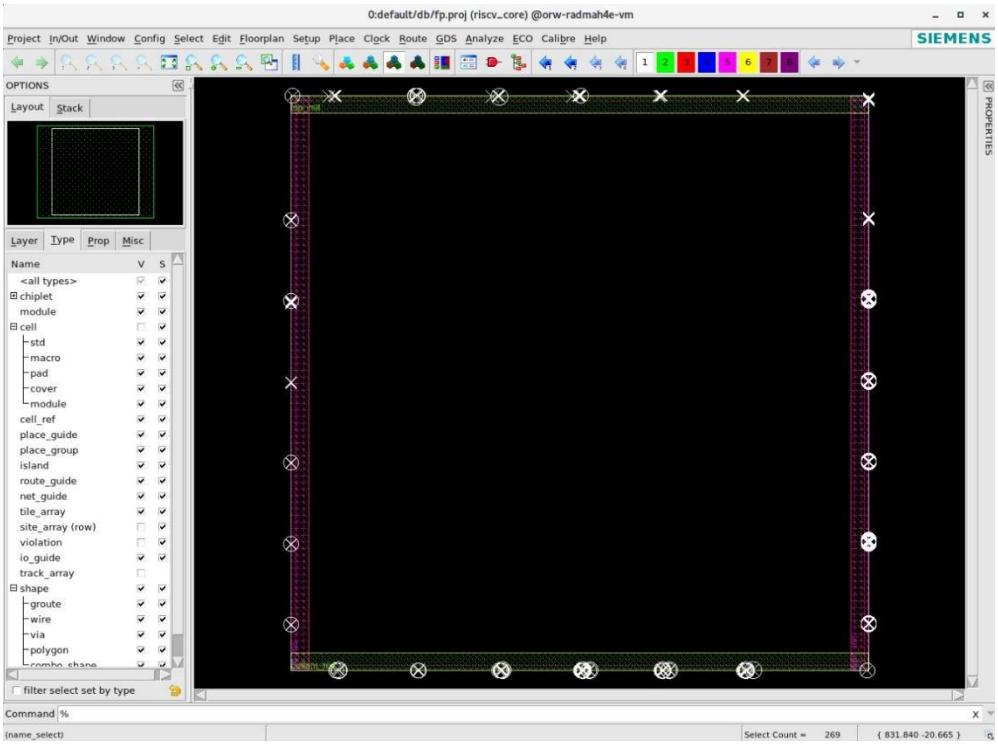

Figure 22: IO pins highlighted in the layout window. (Original)

Step 3 In the ***init_floorplan*** window, enter the following data:

- Select Design Boundary: by_size
- Modify Original Values of: Width : 892.64, Height: 904.96 with Width: 712.880, Height: 718.900

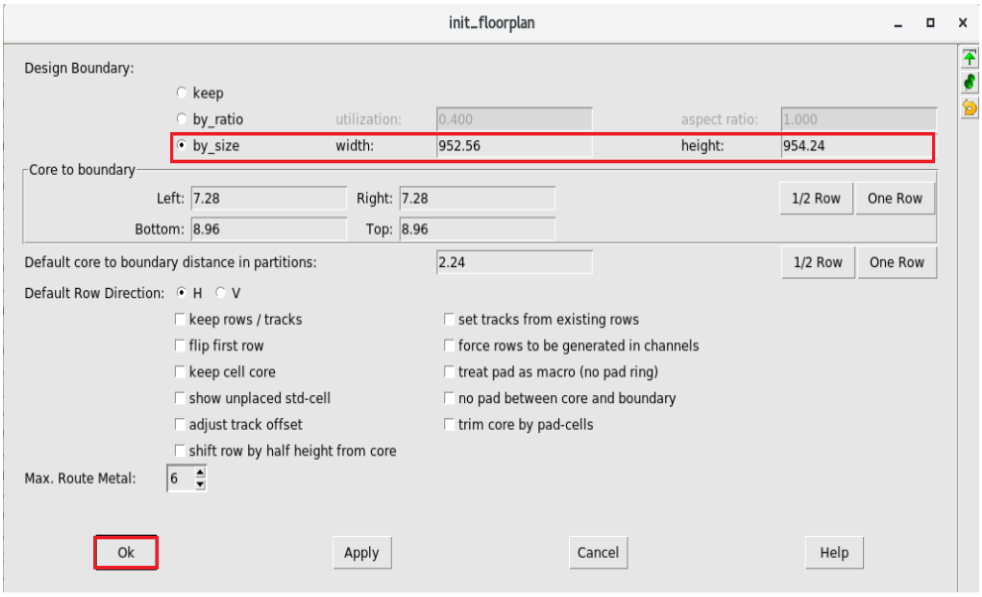

Figure 23: init_floorpan window with floorplan original width and height (Original)

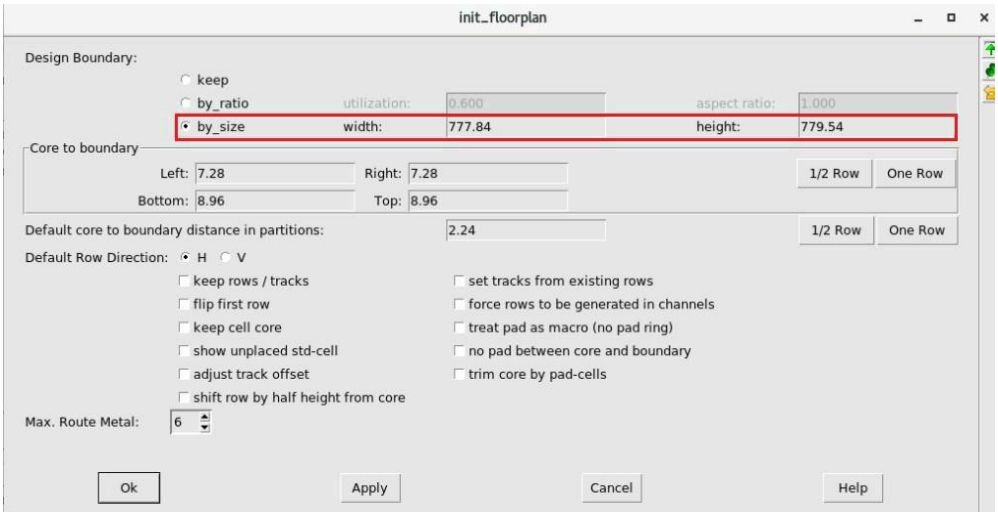

Figure 24: init_floorplan window with floorplan Width and Height (New)

Step 4 Click ***Ok*** button and move back to Aprisa shell session.

Step 5 After new floorplan dimensions, the pins will remain at original location as shown below. To know how to see pin's location, refer to **sub section 5.1.b, go to Step 2,** repeat. **point number 3, Physical Pins Location.**

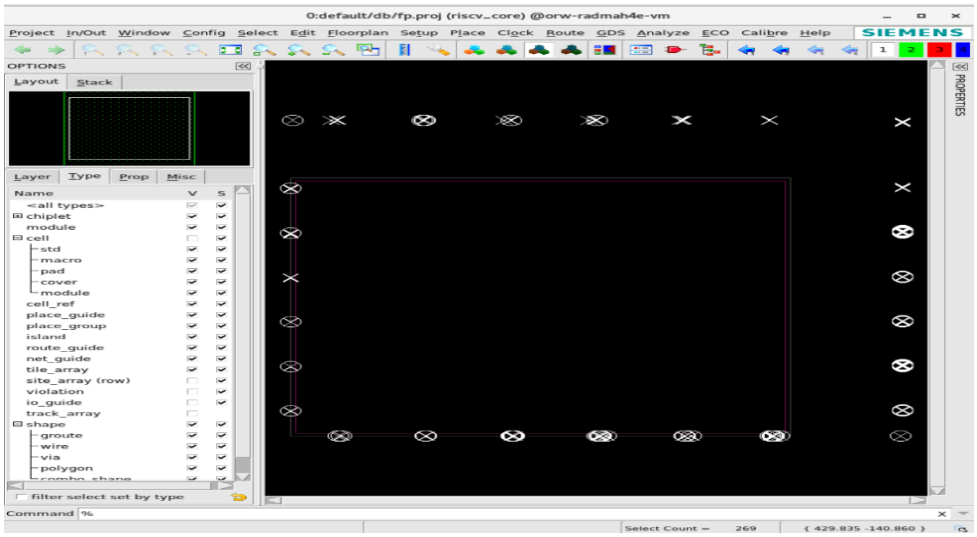

Figure 25: Highlighted IO pins outside of design boundary (Original pin location).

Step 6 **Modify Physical pin location:** Pins need to be relocated as per new floorplan dimensions. To know how to use modify pin's position, refer to **sub section 5.1.b,** repeat **Step 6.**

Step 7 **Observe New values:**
Lastly, measure the utilization ratio, floorplan, physical pin locations of original design.

1. Utilization ratio:

Go to Aprisa shell, use following command to get the present utilization ratio details-

% ***report_placement***

```
utilization
-----------
  die utilization                 =  59.94 % ; C / X
  core utilization                =  62.52 % ; (C - G) / A
  std-cell utilization            =  62.52 % ; D / (A - F)
  placeable-cell utilization      =  62.52 % ; H / B
```

Figure 26: Utilization 60% (New)

2. Measure floorplan dimensions:

Go to APRISA layout window and zoom in to the layout to measure width and height of floorplan using ruler. To know how to use ruler, refer to **sub section 5.1.b** and go to **Step 2,** repeat **point number 2. Measure floorplan dimensions.**

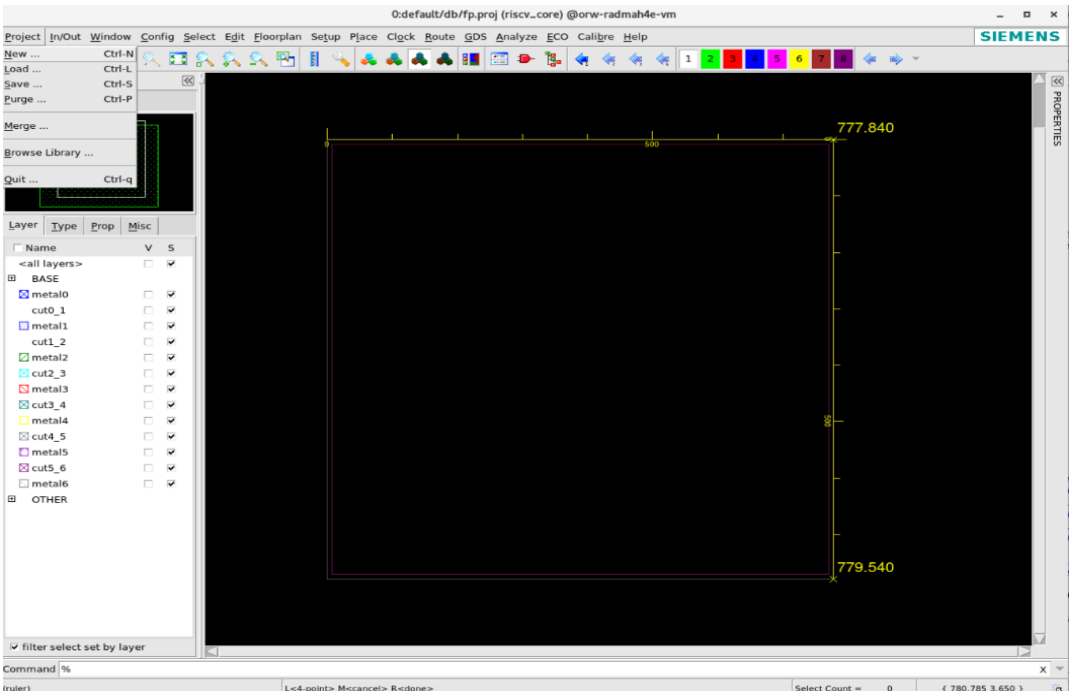

Figure 27: Measurement of height and width of original floorplan (New)

3.Verify the new location of physical pins-

Check the location of physical pins. To know how to verify pin's location, Refer to. **sub section 5.1.b**, go to **Step 2**, repeat **point number 3, Physical Pins Location**

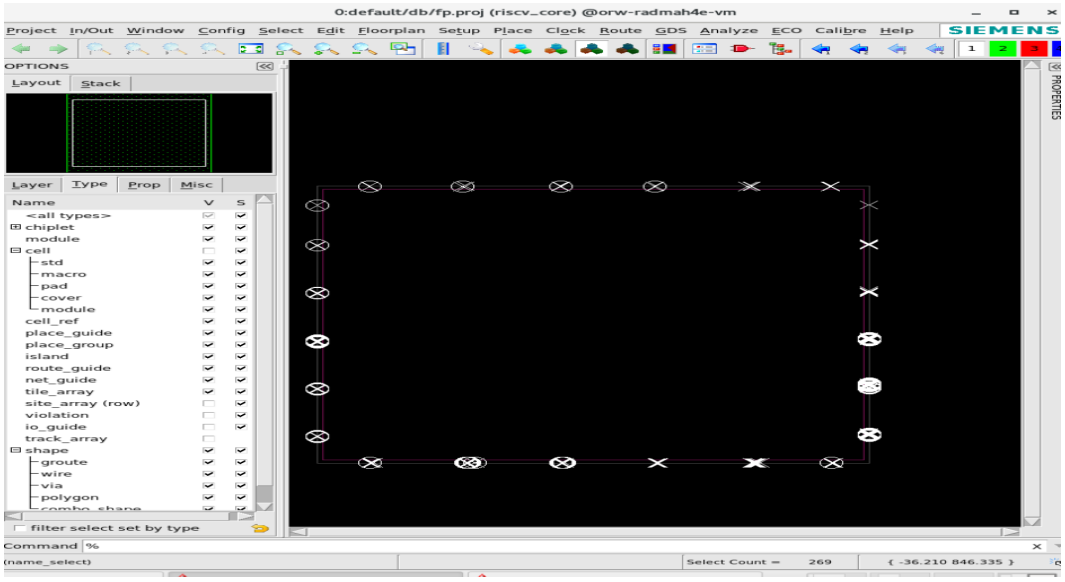

Figure 28: Highlighted IO pins inside the design boundary (New pin location).

Step 8 Exit the current session using the below command:

% exit

5.2.c. TCL Commands

Run the commands either in Command Line Interface (CLI) or Aprisa shell and see the changes in the layout window.

*1.*Load the project in Shell- % ***load_project default/db/fp.proj***

2. Change the utilization ration of floorplan by executing following command:

init_floorplan -boundary by_size -width 777.84 -height 777.84 - max_route_metal 6 --keep_cell_core 3.

To move physical pin location, Go to **Section 5.1.b**, repeat **Step 6.**

4. Observe the changes in the layout window.

5.1.d. Conclusion

In this exercise, it has been demonstrated how to directly minimize design's height and width to reduce die size, using both the GUI and the TCL Command Line Interface (CLI), which ultimately increases the utilization ratio.

Comparison between original and modified floorplan dimensions is shown below:

Width	Height	Utilization ratio
952.56	954.240	39.94 (Original)
777.84	779.540	59.94 (New)

Excerpt: Use any other values of the height and width in ***init_floorplan*** window. Observe how the floorplan is reduced in size and also yields to higher utilization ratio.

5.3. By Keep

x and y co- ordinates of the design layout.

5.3.a. Objective

The objective of this section is to illustrate how to enhance the utilization ratio at the floorplan stage by modifying the x and y co-ordinates of the design using APRISA Tcl commands.

5.3.b. Tcl Commands

Step 1 To load the project, follow the steps mentioned in **Section 4. Getting started.**

Step 2 **Observe Original values:**
To begin, measure the utilization ratio, floorplan, physical pin locations of original design.

1. Report Utilization ratio:
Go to Aprisa shell, get the present utilization ratio details, using following command:

% ***report_placement***

Figure 29: Utilization 40% (Original)

2.Measure floorplan dimensions:
Go to APRISA layout window and zoom in to the layout to measure width and height of floorplan using ruler. To know how to use ruler, refer to **sub section 5.1.b,** go to **Step 2,** repeat **point number 2.**

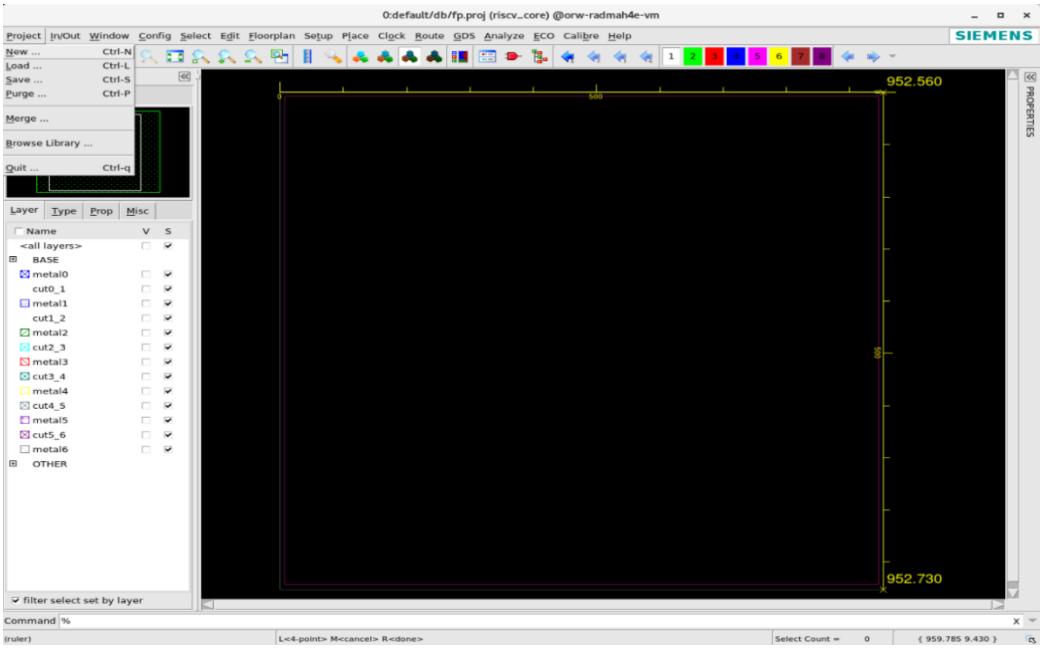

Figure 30: Measured height and width of original floorplan

3.Physical pins location-

Locate the original position of pins. To know how to see the physical pin's location, refer to **sub section 5.1.b,** go to **Step 2,** repeat **point number 3. Physical pin's location.**

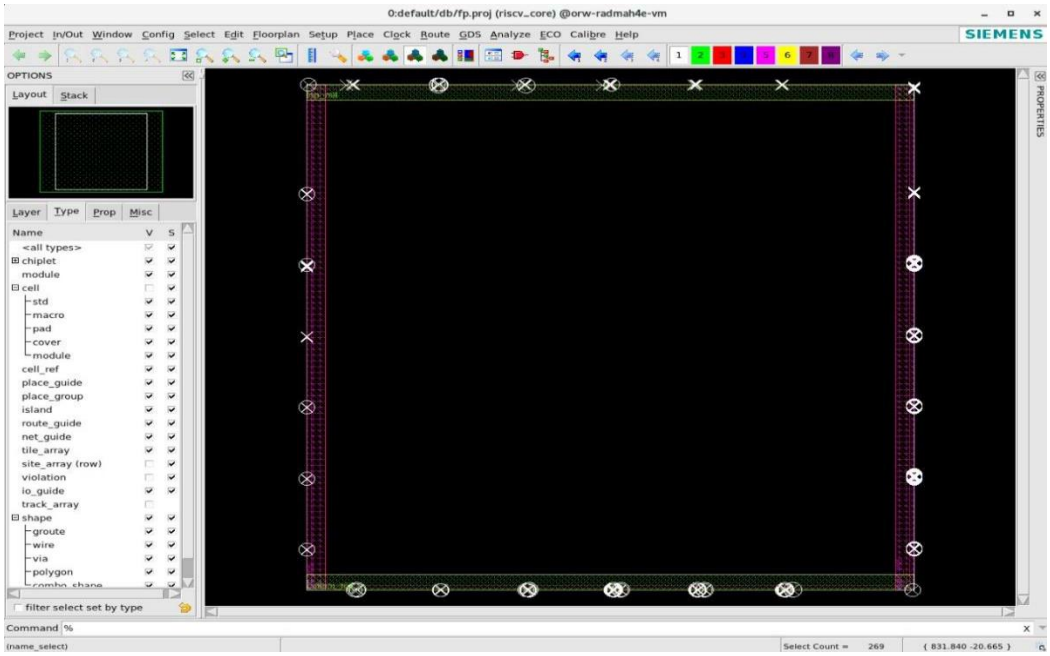

Figure 31: IO pins highlighted in the layout window. (Original)

Step 3 To adjust current values of co-ordinates x and y, use either of the methods mentioned below:

Method 1: Change x and y co- ordinates using command line.

***% set_cell_boundary {} -exclusive -max_route_metal 6 ***

-core_to_boundary {0.000 0.000 777.840 779.540}

set_cell_core {} {7.280 8.960 769.660 770.560}}

Method 2: Change x and y co-ordinates in fp.tcl file-

The x and y co-ordinates of the design can be modified directly in the floorplan file.

- Navigate to the Aprisa shell. To begin with, export floorplan setup of design using command:

  %export_setup <my_floorplan. fp>

- Navigate to working directory where exported floorplan file is saved as my_floorplan.fp.

- Open the file using command-

  % / gvim my_floorplan.fp

- A dialog box will appear. Click "Edit anyway" at the bottom to indicate that the file. can be modified.

Figure 32: Dialog-box asking file permission.

- Once, file is opened, find the floorplan boundary. Enter insert mode by pressing the Insert key, and observe the highlighted INSERT keyword at the bottom, indicating the file can be overwritten.

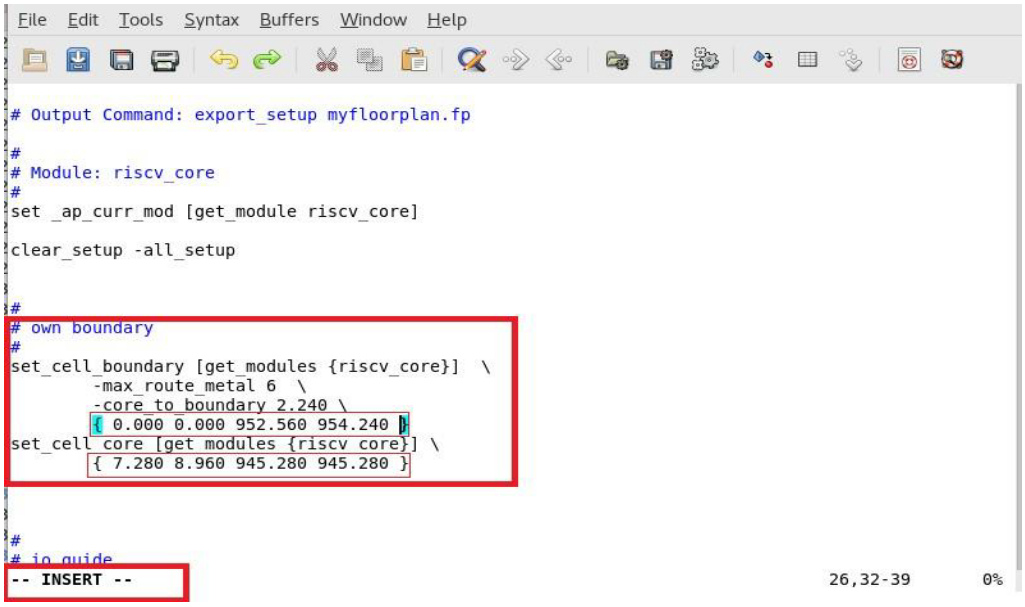

Figure 33: Floorplan details in my_flooplan.fp file

- Now, modify original coordinate values with new values shown below:

```
set_cell_boundary [get_modules {risc_core}] \
        -max_route_metal                6                       \
        -core_to_boundary 2.240 \
       {{0.000          0.000          777.840          779.540}
set_cell_core [get_modules {risc_core}] \
              {7.280 8.960 769.440 770.560}
```

- After modifying values, click on file option in top left corner, select ***Save- Exit*** option shown below.

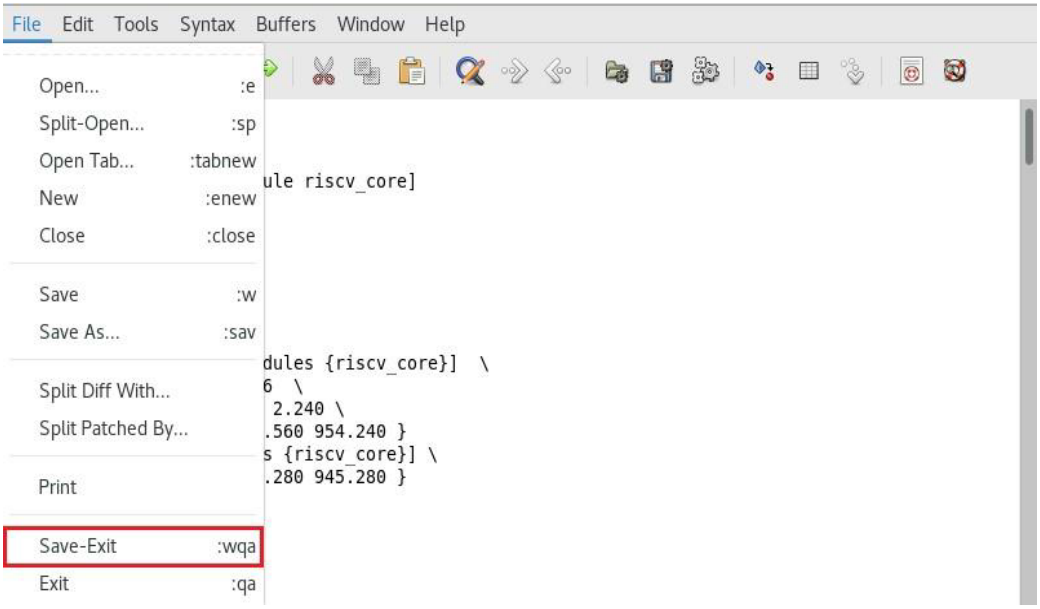

Figure 34: Save-Exit my_flooplan.fp file

Step 4 Go to shell, invoke AP in the working directory:

%AP

Step 5 Load already saved project using the command:

% ***load_project default/db/fp.proj.***

Step 6 Source my_floorplan.tcl file with new floorplan values using command:

% ***<working directory> source my_floorplan.tcl***

Step 7 After, my_floorplan.tcl is sourced, initialize floorplan using command:

% init_floorplan -boundary keep -keep_cell_core -max_route_metal 6

Step 8 After new floorplan dimensions, the pins will remain at original location as shown below. To know how to see pin's location, refer to **sub section 5.1.b, go to Step 2,** repeat **point number 3, Physical Pins Location.**

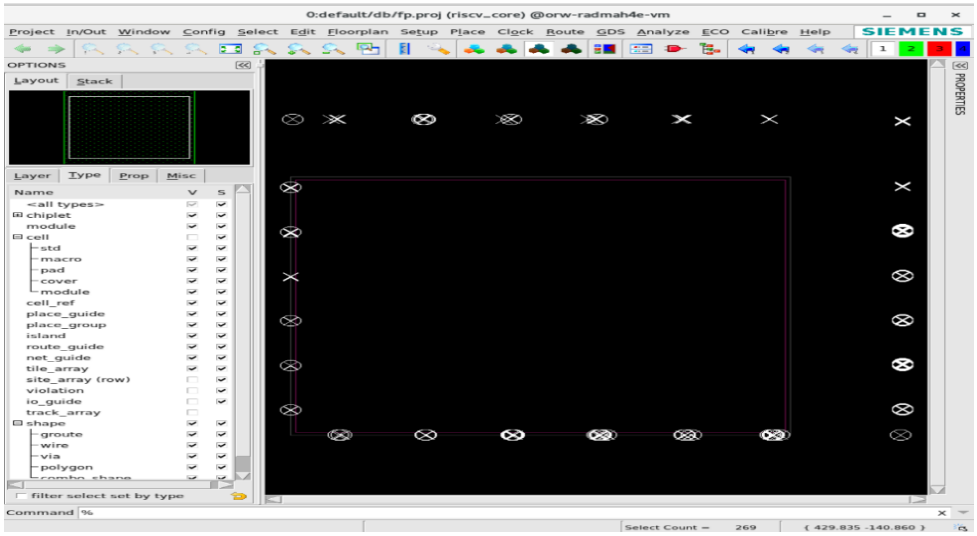

Figure 35: Highlighted IO pins outside of design boundary (Original pin location).

Step 9 **Modify Physical pin location:** Pins need to be relocated as per new floorplan dimensions. To know how to use modify pin's position, refer to **sub section 5.1.b,** repeat **Step 6.**

Step 10 **Observe New values:**

Lastly, measure utilization ratio, floorplan, physical pin locations of original design.

1. Utilization ratio:

Go to Aprisa shell, use following command to get the present utilization ratio details-

% ***report_placement***

```
utilization
-----------
  die utilization                =  59.94 % ; C / X
  core utilization               =  62.52 % ; (C - G) / A
  std-cell utilization           =  62.52 % ; D / (A - F)
  placeable-cell utilization     =  62.52 % ; H / B
```

Figure 36: Utilization 40% (Original)

2. Measure floorplan dimensions:

Go to APRISA layout window and zoom in to the layout to measure width and height of floorplan using ruler. To know how to use ruler, refer to **the sub section. 5.1.b** and go to **Step 2,** repeat **point number 2. Measure floorplan dimensions.**

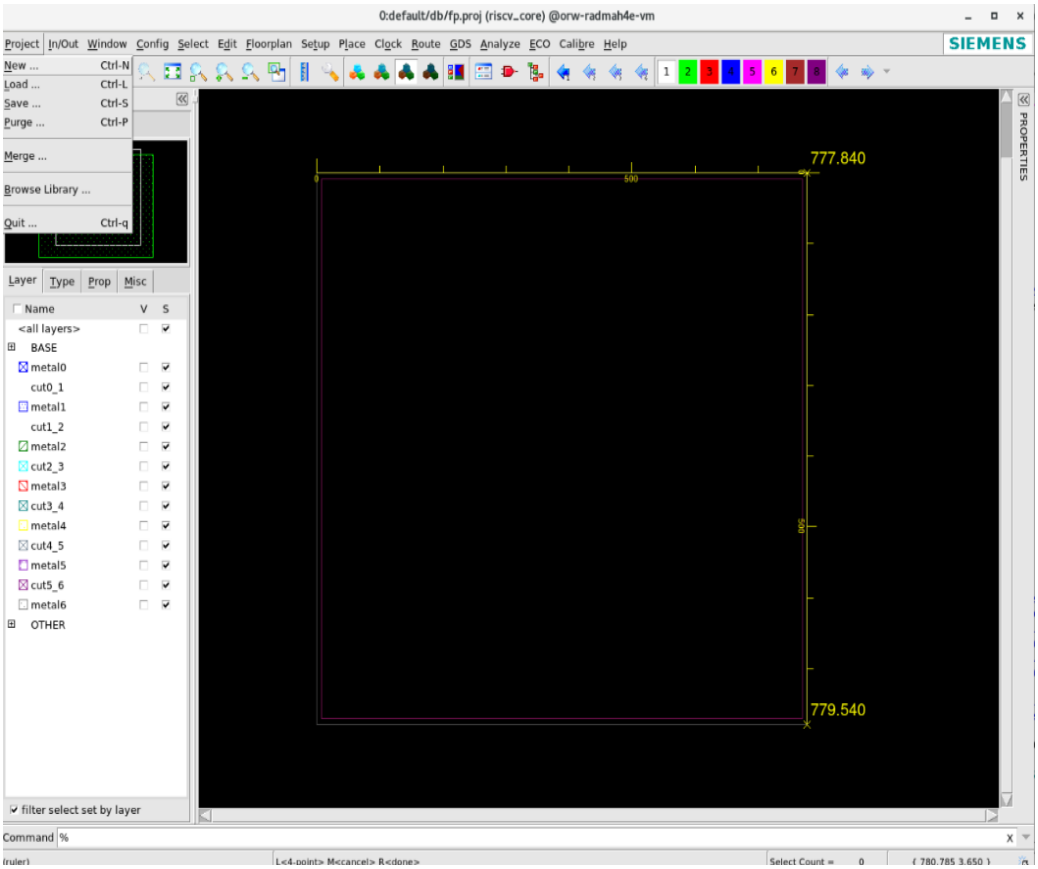

Figure 37: Measurement of height and width of original floorplan (New)

3.Verify the new location of physical pins-

Check the location of physical pins. To know how to verify pin's location, Refer to. **sub section 5.1.b**, go to **Step 2**, repeat **point number 3, Physical Pins Location**

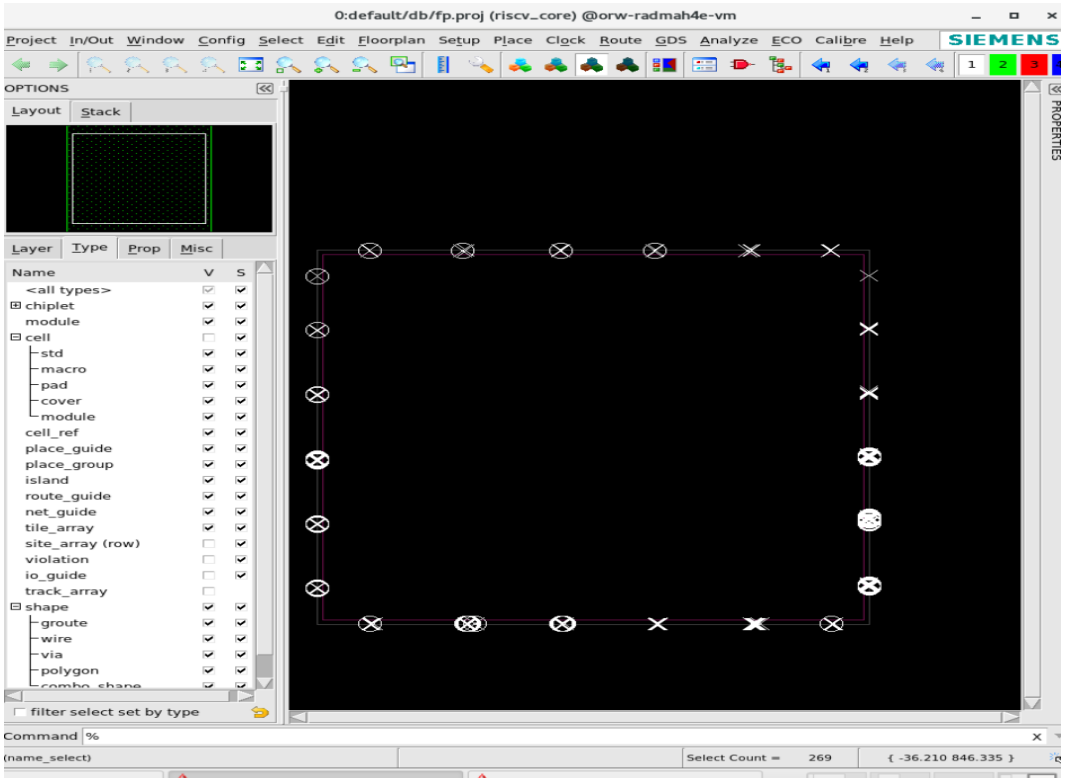

Figure 38: Highlighted IO pins outside of design boundary (New pin location)

Step 11 Exit the current session using the below command:

% exit

5.3.c. Conclusion

In this exercise, it has been demonstrated how to reduce the x and y coordinate values using the TCL Command Line Interface (CLI), ultimately enhancing the utilization ratio and reducing die size at floorplan stage.

Comparison between original and modified floorplan dimensions is shown below:

Boundary Co-ordinates	Core co-ordinates	Utilization ratio
{0.000 0.000 952.560 954.240}	{7.280 8.960 945.280 945.280}	39.94 (Original)
{0.000 0.000 777.840 779.540}	{7.280 8.960 769.660 770.560}	59.94 (New)

Excerpt: Experiment using any other smaller values for co-ordinates for the boundary and core values. Observe how the floorplan is reduced in size, higher utilization ratio.

7. Conclusion

1. Reduction in size of die

Instead of occupying more space, cells are placed more closely and efficiently in the core area, ultimately leading to smaller sized chips.

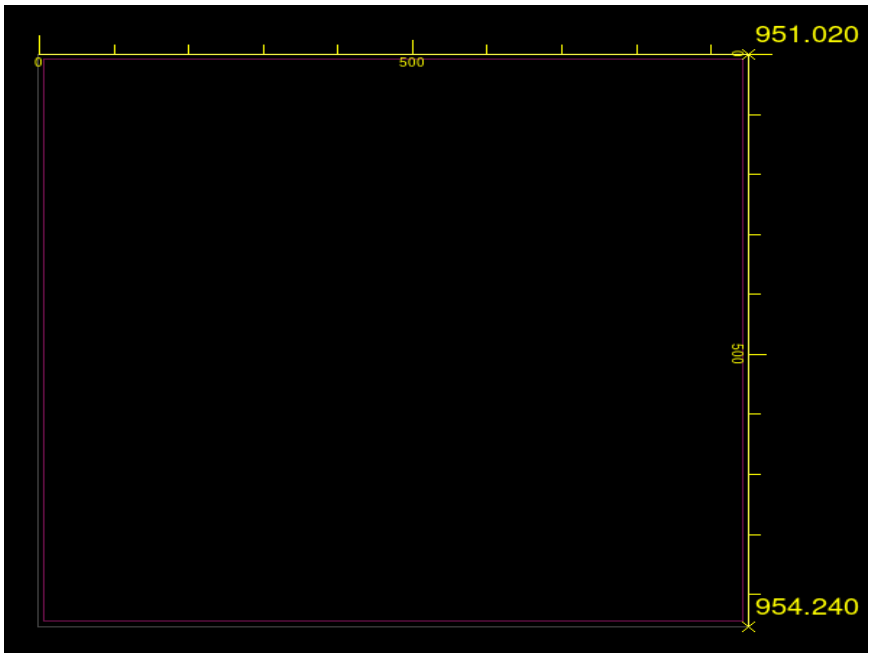

Figure 39: Die size for Utilization ratio 0.40 (Original)

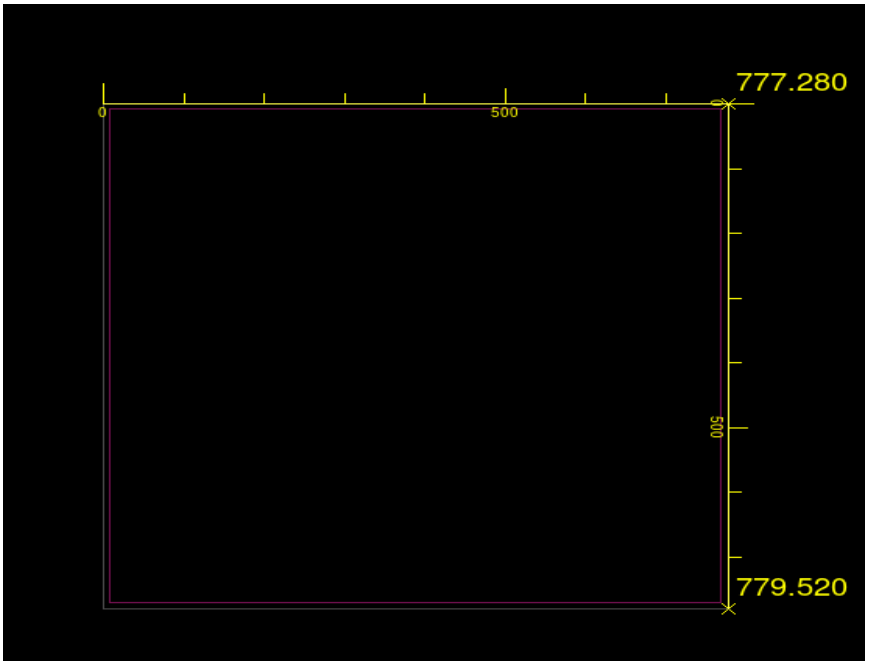

Figure 40: Die size for Utilization ratio 0.60 (New)

2. Efficient placement of standard cells.

Utilization ratio also affects the standard cell placement. Thus, during the placement stage, differences in the placement of standard cells become apparent due to different utilization ratios.

Therefore, out of curiosity, users may attempt to run the placement stage and analyse the ***placement differences of standard cells*** for both original and new ratios of 0.40 and 0.60 as shown below:

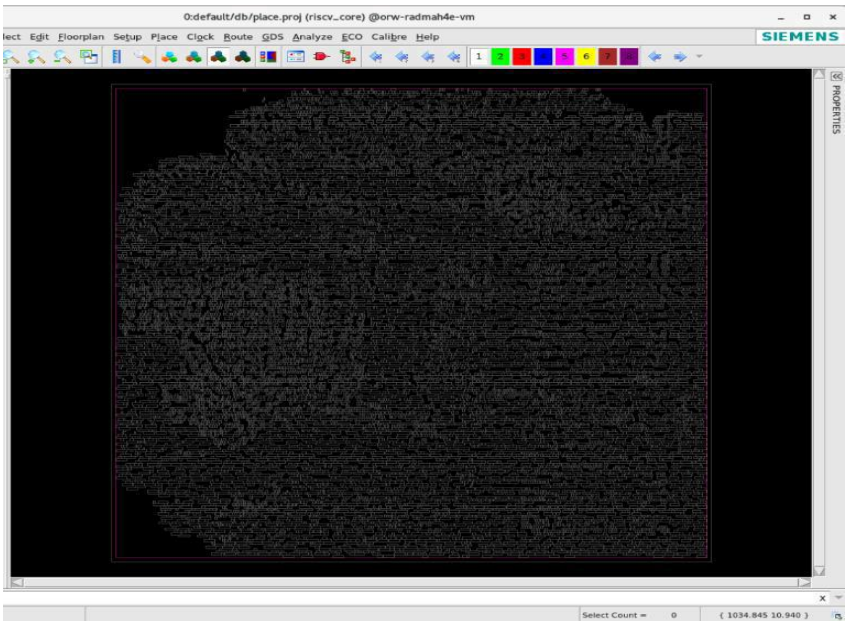

Figure 41: Standard cell placement, utilization ratio 0.40 (Original)

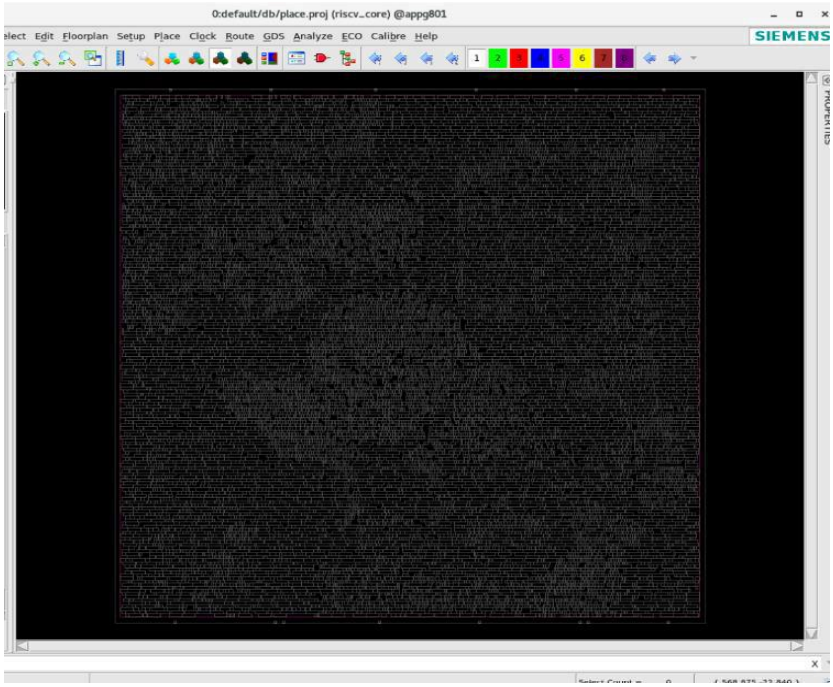

Figure 42: Standard cell placement, utilization ratio 0.60 (New)