Effective downsampling techniques for SEM defect inspection using design insights in machine learning

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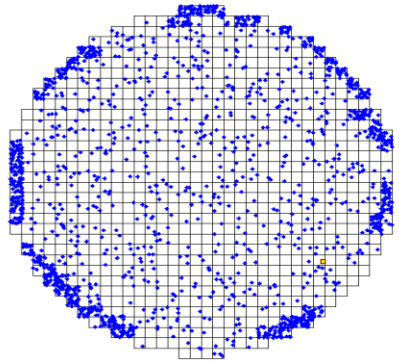
Outline

- Introduction
- Methodology
- Experiments and Results
  - Process Window Qualification
  - ROI (Return-Of-Investment)
- Conclusion

Introduction to wafer defect down sampling flow

BFI defect inspection → Defect down sampling → SEM defect review → Defect classification & analysis

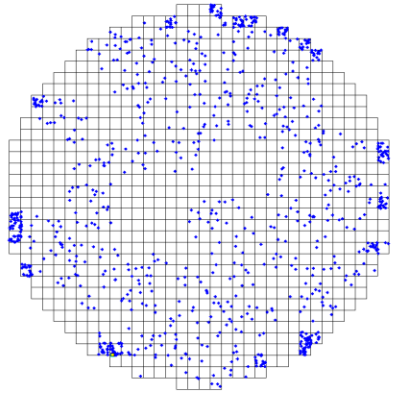
Defect Wafer map
Reports approx. ~100,000 defects



- Fast, full wafer inspection;
- Optical image pixel size ~10x nm

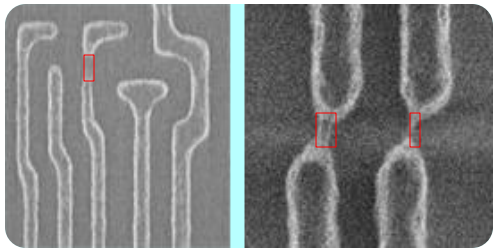
Effective down sample enables:
- Increase hit rate
- Accurate defect performance analysis

Defect Wafer map
Review approx. ~1,000 defects



- Slow, image taken on selected locations;
- SEM image pixel size ~1x nm

Classified SEM defects

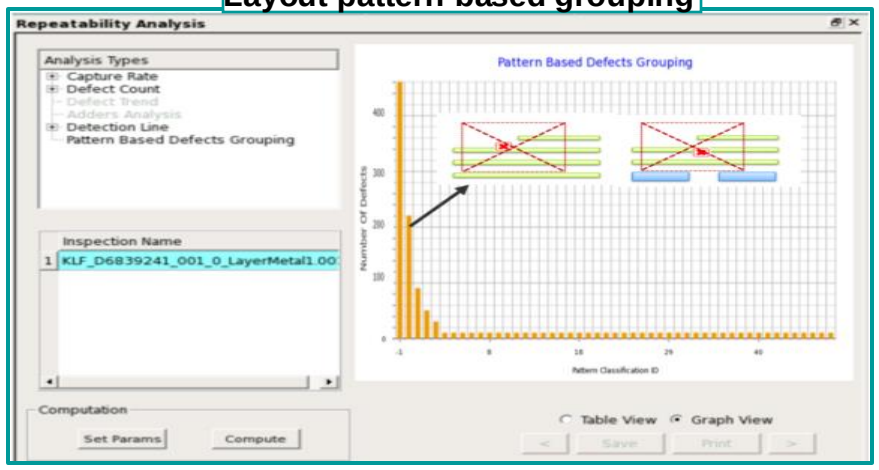


Methodology
-- Defect down sample with design and process information

- Design systematics in wafer manufacturing:
  - Design systematics are often seen in R&D stage of new tech node development
  - Process and design systematics can happen during yield ramp up even HVM, especially on wafer edge dies

- Defect down sampling in Calibre Wafer Defect Management (GUI based):
  - Layout pattern based: perform pattern-based defect grouping, sample as many pattern variety as possible
  - Machine learning based (integrating Calibre SONR): with features not limited to layout geometry, but various design/process/defect signal features, sample based on selected feature group similarity

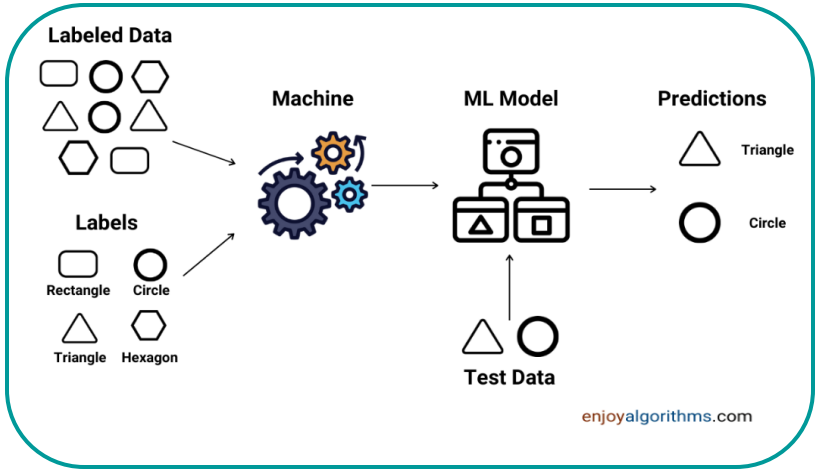
Layout pattern based grouping



Machine learning methods in Calibre SONR

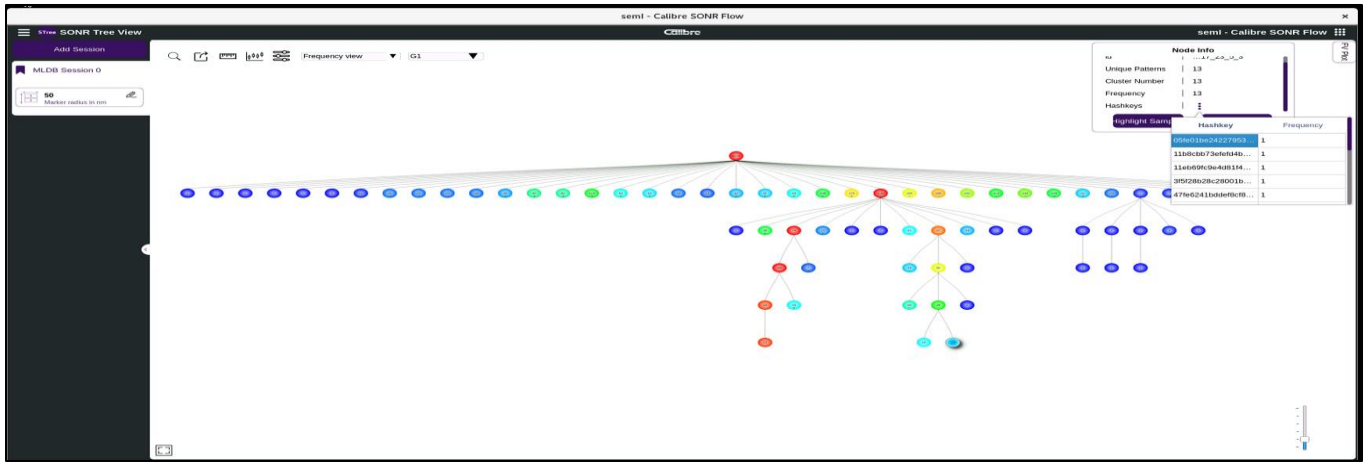
Supervised ML

Labeled data



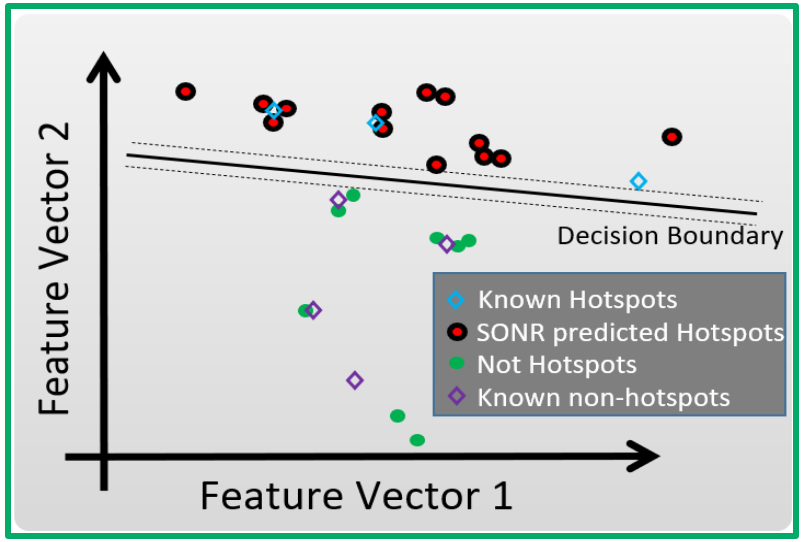
Un-supervised ML

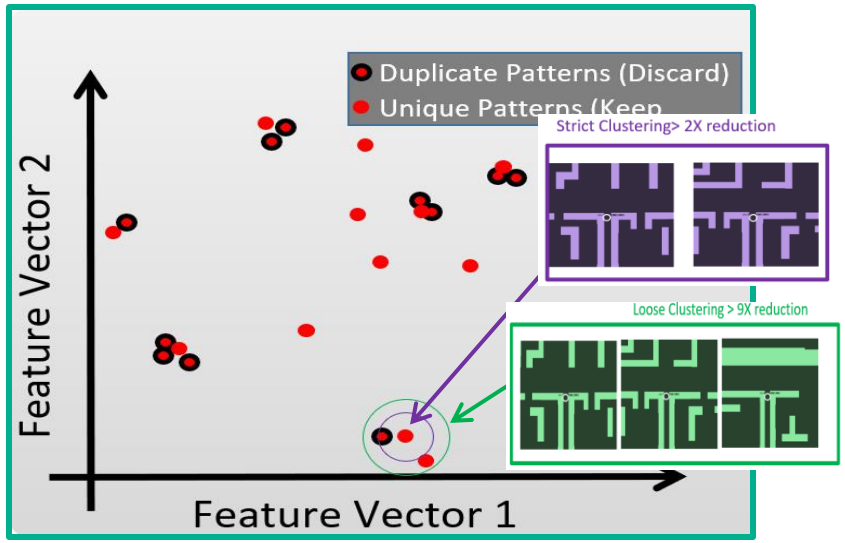
No labeled data

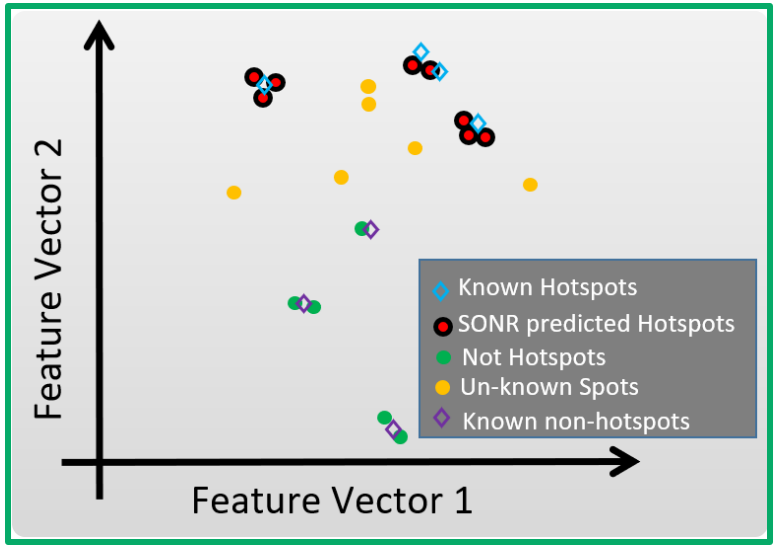


Semi-supervised ML

Combination of labeled & unlabeled data

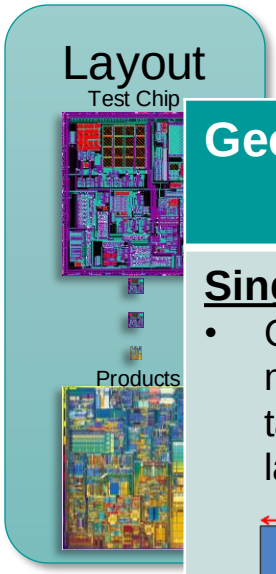






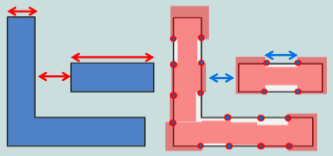
Calibre SONR feature engineering

- Feature Engineering is one of the most critical tasks in success with ML applications.
- Internal SONR features include layout and process information
- Allows users to define their own custom features easily

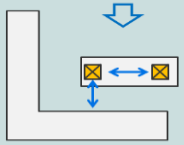


Geometry

Single layer:
- Geometry measurements on target layer/retarget layer/ opc layer

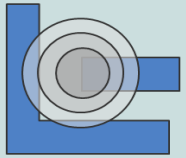


Multiple layers:
- Geometry measurement between the layers, e.g. via and metal.

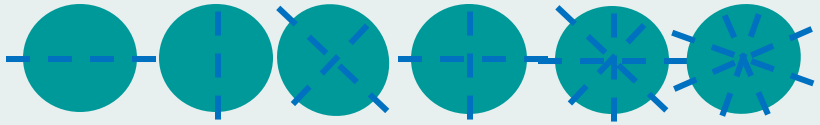


Density

Short range un-directional:
- Short range up to 1-5um
- Tophat and Gaussian with customer setup



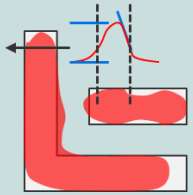
Short range directional:
- Split the kernel into 2/4/8 sections.



Long range
- Long range density up to 1mm.
- Include Tophat and Gaussian
- Include un-directional and directional

Process

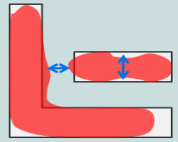
Intensity terms:
- Include Imin/Imax/ slope of the intensity
- Include resist/DDM



Optical terms:
- Calculate the optical information from the optical model only.
- Siemens IP.

Others

OPCV features:
- Contour information
- OPCV checks
- VEB features

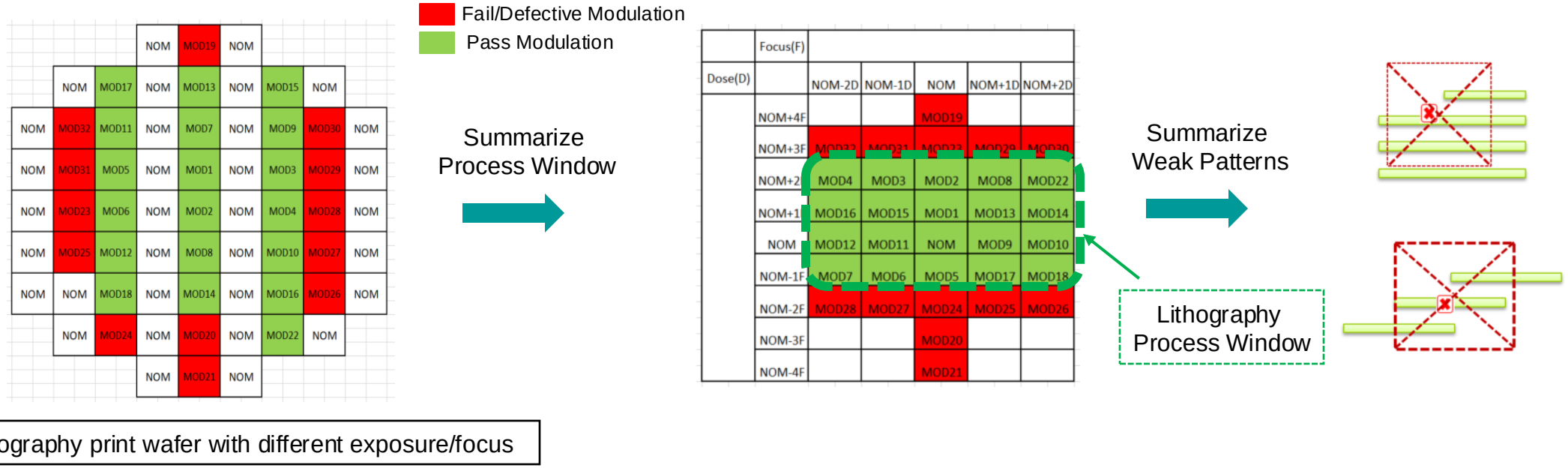


DFM properties:
- Any DFM properties defined by the users

PNG map:
- Value saved in png map

Experiments and Results

- Process Window Qualification



Customer A: using both Pattern based + ML down sampling *vs* fab POR
Customer B: using only ML down sampling *vs* fab POR

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Benchmark results

Customer A[1]

PWQ analysis Dataset 1	Baseline	Pattern based + Machine Leaning
Defect Hit Rate	1x	2x
# of Systematic Weak Patterns	1x	4x
# of Failing Process Windows	1x	1.25x

PWQ analysis Dataset 2	Baseline	Pattern based + Machine Leaning
Defect Hit Rate	1x	36x*
# of Systematic Weak Patterns	1x	57x*
# of Failing Process Windows	1x	2x

*note that dataset 2 has large improvements as the POR method sampled a large number of nuisance defects of same pattern

Customer B[2]

PWQ analysis	Baseline	Machine Learning
Defect Hit Rate	1x	40x
# of Systematic Weak Patterns	1x	6x
# of Failing Process Windows	1x	1.5x

[1] J. Jiang et al., "Reducing Systematic Defects using Calibre Wafer Defect Engineering and Machine Learning Solutions," 2020 International Workshop on Advanced Patterning Solutions (IWAPS)

[2] Y.Ma, J Optiz et al, “Cross produces hotspot detection with Calibre SONR: A machine learning technique” 2020, DAC conference

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ROI (Return-Of-Investment)

<table>
<tr><th rowspan="2">Proposed method technical benefits</th><th colspan="2">ROI Calculation</th></tr>
<tr><th>Volume production</th><th>R&D Development</th></tr>
<tr><td>Higher SEM defect hit rate with lower SEM review defect count

Customer POR: 1x
Proposed method:2x</td><td colspan="2">Save tool time for additional rounds of SEM review/inspection but achieve same defect discovery goal;
Less review means engineer time saved for defect analysis</td></tr>
<tr><td rowspan="2">Discovery more weak patterns with less rounds of SEM review/defect inspection

Customer POR: 1x
Proposed method:4x</td><td>Expedite volume production of customers with multiple products (common IP→solve 1 product, benefits many);</td><td>Expedite development cycle by reducing mask re-spin rounds which save significant amount of money and time;</td></tr>
<tr><td>Reduce yield loss by reducing design systematics which makes each wafer more profitable;
Reduce reliability issues</td><td>Decrease yield ramp up time</td></tr>
</table>

Conclusion

- Proposed pattern based + machine learning based defect down sampling flow

- Experiments shows the proposed flow provides：
  - Increased defect hit rate
  - More accurate lithography process window
  - More systematic pattern varieties found

- Return-Of-Investment analysis shows proposed method benefits in:
  - Tool and engineer time saving
  - Mask re-spin reduction and yield improvements
  - Yield ramp up acceleration and reliability issue reduction

Thank you!

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