

SIEMENS EDA



How to Extract Parasitic Inductance using Calibre xL

2024.2

Outline



- Objective
- Included Files
- Description
- Directions
- Conclusion

Objective



This Support Kit should help you understand how to:

- Understand the different use models and modes (PEEC/LOOP) that are supported in Calibre xL
- Use LOOP mode to extract Block level RCCLM
- USE PEEC mode to extract Block level RCC, and select critical nets RCCLM
- Extract a single RCCLM netlist in the same PEX run

Included Files

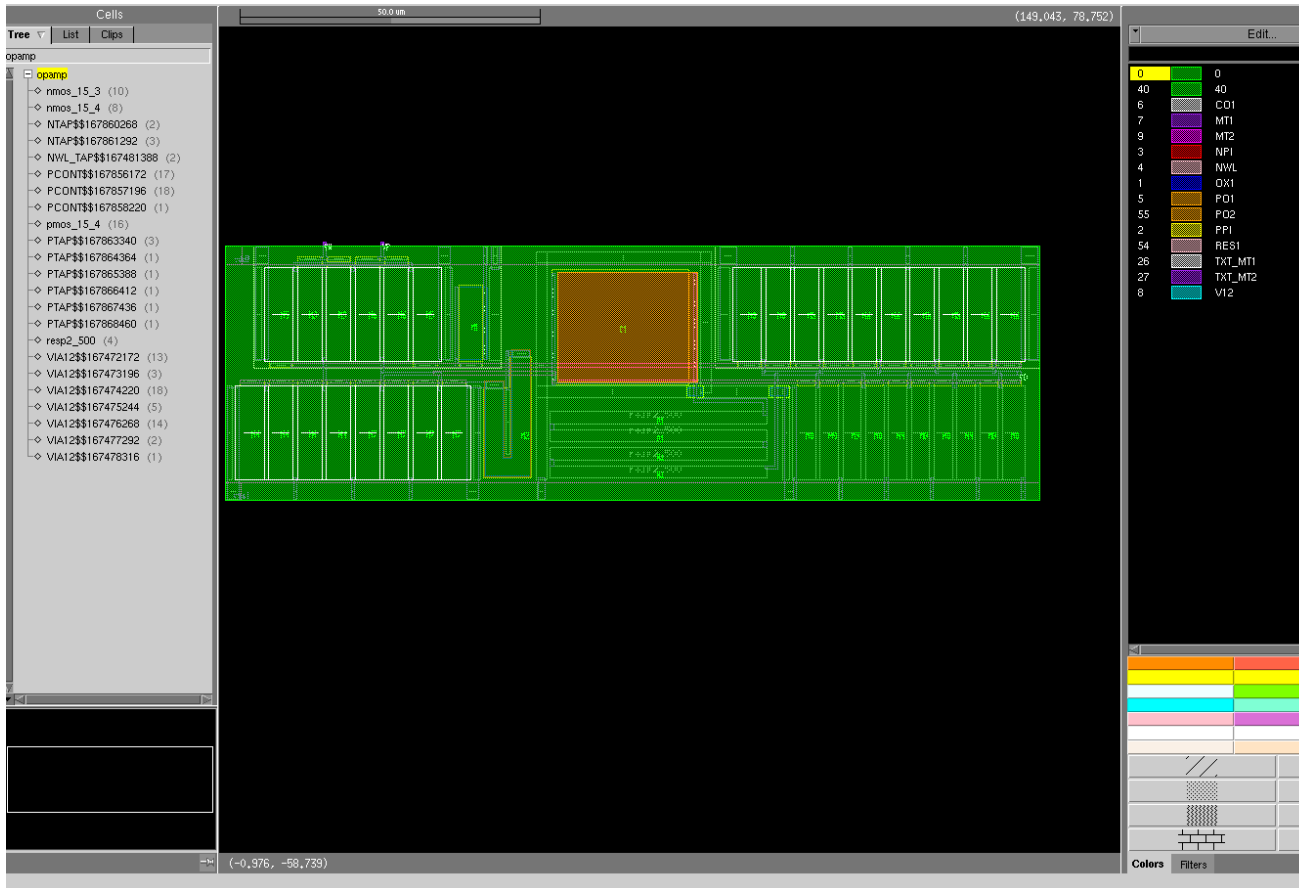
File	Description
layout.gds	Sample GDS file
layout.gds.layerprops	Layer properties file to annotate the layer names
opamp.src.net	Sample spice netlist
runme	Script to run Calibre xRC
top.rules	top level rule deck that contains inductance rules
rules.pex	Parasitic capacitance rule deck
rules.lvs	LVS rule deck
rules.C	Calibrated Parasitic capacitance rule deck
rules.R	Calibrated Parasitic resistance rule deck
rules.xact	Calibrated Parasitic rule deck for xACT
mv-results.csh	Script to move the results of each run into the designated directory
cleanme	Script to clean up the run directory

Description

>> Layout

View the sample layout file with the command:

```
calibredrv layout.gds
```



After examining the layout close
Calibre DESIGNrev

Description

- Inductance parasitics occur due to the magnetic field generated by currents passing through conductors. These parasitics can impact on chip performance including signal delay, ringing, and overshooting
- Calibre xL provides a fast and accurate field solver-based inductance extraction engine to extract both self and mutual inductance parasitics of on-chip interconnects.
- Calibre xL is fully integrated with xRC, xACT and xACT3D to generate a single RCCLM netlist in a single PEX run.
- Calibre xL supports two modes: **LOOP** and **PEEC**
- **LOOP** mode is associated with the extraction of loop self and mutual inductance for signal/return-path current loops in the layout. Only signal wires are represented in the netlist using the loop approach. The return path nets (PWR/GND) inductance values are included with the signal net values .
- **PEEC mode** is associated with the extraction of parasitic “inductance” for straight wire segment. Both signal and ground segments, if selected, are represented in the netlist separately.

Description

Pre-requisites for running Calibre xL

1. Calibre qualified deck with xRC , xACT, or xACT3D
2. Define extraction use model:
 - Block level RCC, and select critical nets RCCLM (LOOP or PEEC)
 - Block level RCCLM (LOOP mode)
3. Define the inductance extraction mode through **PEX INDUCTANCE MODE LOOP|PEEC**
4. Define the extraction frequency through **PEX INDUCTANCE FREQUENCY**
 - LOOP can be run on a single frequency or across a broadband model
 - PEEC can only be run on a single frequency

Description

>> Rule Deck

```
#IFDEF $MODE LOOP
PEX INDUCTANCE MODE LOOP
PEX POWER SOURCE "vdd!"
PEX GROUND SOURCE "vss!"
PEX INDUCTANCE RETURNPATH GANDP
PEX INDUCTANCE RANGE 10
#ENDIF
#IFDEF $MODE PEEC
PEX INDUCTANCE MODE PEEC NETS SOURCENAMES "VP" "VN" "VO"
#ENDIF

PEX INDUCTANCE MINLENGTH 10
PEX INDUCTANCE MAXIMUM FREQUENCY 5000000000
```

Only part of the rule deck is shown in this slide

The rule deck supports 2 runs: LOOP and PEEC

- For LOOP mode the following must be defined:
 - The power and ground nets using **PEX GROUND** and **PEX POWER**
 - The return path for the signal nets for self impedance calculations using **PEX INDUCTANCE RETURNPATH**
 - The search distance from net segments to look for the return paths using **PEX INDUCTANCE RANGE**
- For PEEC mode you must specify the nets of interest for inductance extraction using **PEX INDUCTANCE MODE PEEC NETS**

Description

>> runme

```
#!/bin/csh -f

setenv MODE LOOP
calibre -lvs -hier top.rules |& tee lvs.log
calibre -xact -rcclm top.rules |& tee xact.log
mv-results.csh

setenv MODE PEEC
calibre -lvs -hier top.rules |& tee lvs.log
calibre -xact -rcclm top.rules |& tee xact.log
mv-results.csh
```

- runme file invokes 2 Calibre xACT runs:
 - With “MODE” = LOOP, it will run in LOOP mode, with the necessary settings on all the nets in the design
 - With “MODE” = PEEC, it will run PEEC mode on selective nets
- After every run, runme file invokes the mv-results.csh scripts, which:
 - Renames the svdb and output netlist with respect to RUN_TYPE variable: svdb.\${MODE} and netlist.dspf.\${MODE}
 - Creates a directory with the MODE variable name and moves the database, netlist and log files into it

Directions

- From the terminal, execute the runme file:

```
source ./runme
```
- For the coming section, you will be directed into opening the following, created by each run
 1. The Standard Verification Database (SVDB) through Calibre Results Viewing Environment (RVE)
 2. xACT log files using any text editor
- Please make sure that you close the RVE after each results view in order to proceed to the next step: viewing the SVDB of the next run in-line

Directions

>> Results LOOP mode

- Open the log file of LOOP run: LOOP/xact.log
- Look for “INDUCTANCE EXTRACTION OPTIONS” in the opened log file
- Notice The Following:
 - A warning message is issued that no victim nets are found for mutual inductance calculations
 - All the inductance extraction settings for the run are reported
 - The vss! and vdd! were recognized as return paths for the signal nets

```
WARNING: No victim net paths for mutual inductance calculations could
be established. Please make sure a PEX INDUCTANCE VICTIM statement is
present in the rule file.
```

```
-----
----                               INDUCTANCE EXTRACTION OPTIONS
-----
```

```
-----
Extraction Mode                : LOOP
Default global frequency (Hz)  : 5e+09
Inductance range (um)          : 10
Minimum length to compute self L (um) : 10
Return Path Mode                : GANDP
```

```
WARNING: Missing/incomplete profile definition for layer PTAP - layer
ignored
WARNING: Missing/incomplete profile definition for layer NTAP - layer
ignored
WARNING: Missing/incomplete profile definition for layer P02_nores - l
ayer ignored
```

```
INFO: Return path nets found :
vss!
vdd!
```

LOOP mode needs Victim nets to be specified in order to extract mutual inductance. Victim nets are defined using **PEX INDUCTANCE VICTIM**

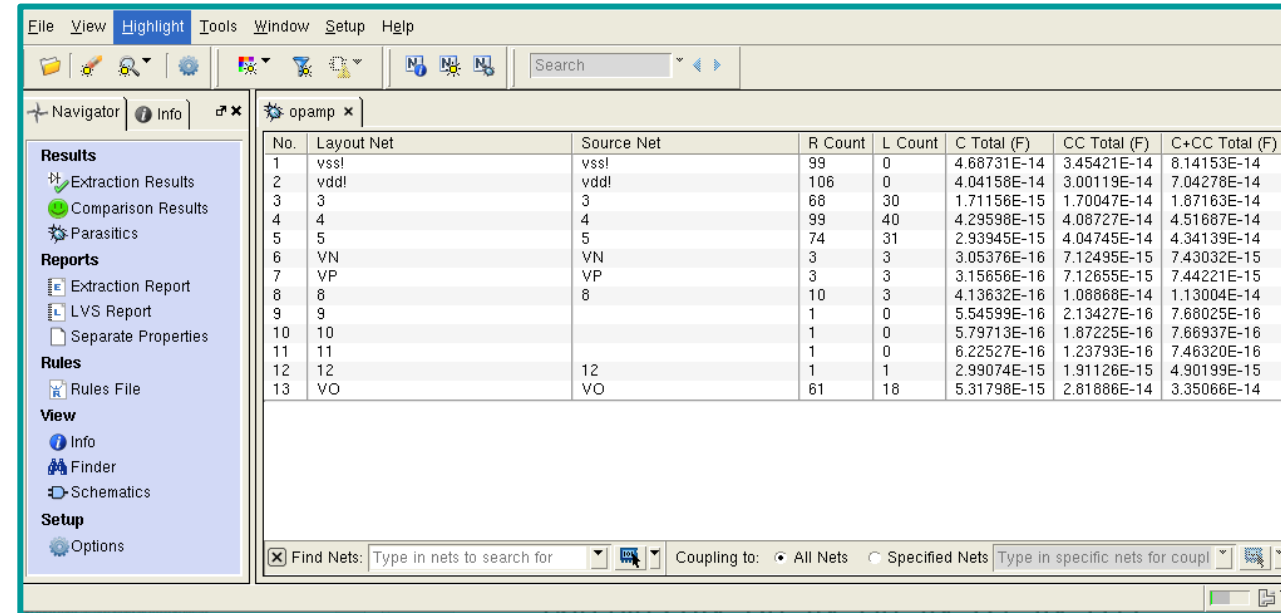
Directions

>> Results LOOP mode

- From the terminal, invoke Calibre RVE with the svdb created from the **LOOP** mode run:

```
calibre -rve LOOP/svdb.LOOP
```

- Notice The Following:
 - Parasitic Inductance for all signal nets is extracted
 - Since vss! and vdd! were recognized as return paths for the signal nets, their inductance values are included in the calculated inductance loop for signal net
 - No mutual inductance is extracted for any of the nets
 - Parasitic caps are extracted for all nets



No.	Layout Net	Source Net	R Count	L Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	vss!	vss!	99	0	4.68731E-14	3.45421E-14	8.14153E-14
2	vdd!	vdd!	106	0	4.04158E-14	3.00119E-14	7.04278E-14
3	3	3	68	30	1.71156E-15	1.70047E-14	1.87163E-14
4	4	4	99	40	4.29598E-15	4.08727E-14	4.51667E-14
5	5	5	74	31	2.93945E-15	4.04745E-14	4.34139E-14
6	VN	VN	3	3	3.05376E-16	7.12495E-15	7.43032E-15
7	VP	VP	3	3	3.15656E-16	7.12655E-15	7.44221E-15
8	8	8	10	3	4.13632E-16	1.08868E-14	1.13004E-14
9	9		1	0	5.54599E-16	2.13427E-16	7.68025E-16
10	10		1	0	5.79713E-16	1.87225E-16	7.66937E-16
11	11		1	0	6.22527E-16	1.23793E-16	7.46320E-16
12	12	12	1	1	2.99074E-15	1.91126E-15	4.90199E-15
13	VO	VO	61	18	5.31798E-15	2.81886E-14	3.35066E-14

Directions

>> Results PEEC mode

- Open the log file of PEEC run: PEEC/xact.log
- Look for “INDUCTANCE EXTRACTION OPTIONS” in the opened log file
- Notice The Following:
 - The selected nets that were specified for the PEEC run are reported
 - All the inductance extraction settings for the run are reported

```
Selected nets:
  net VN
  net VP
  net V0
```

```
-----
-----
-----
INDUCTANCE EXTRACTION OPTIONS
-----
-----
```

```
Extraction Mode           : PEEC
Default global frequency (Hz) : 5e+09
Minimum length to compute self L (um) : 10
```

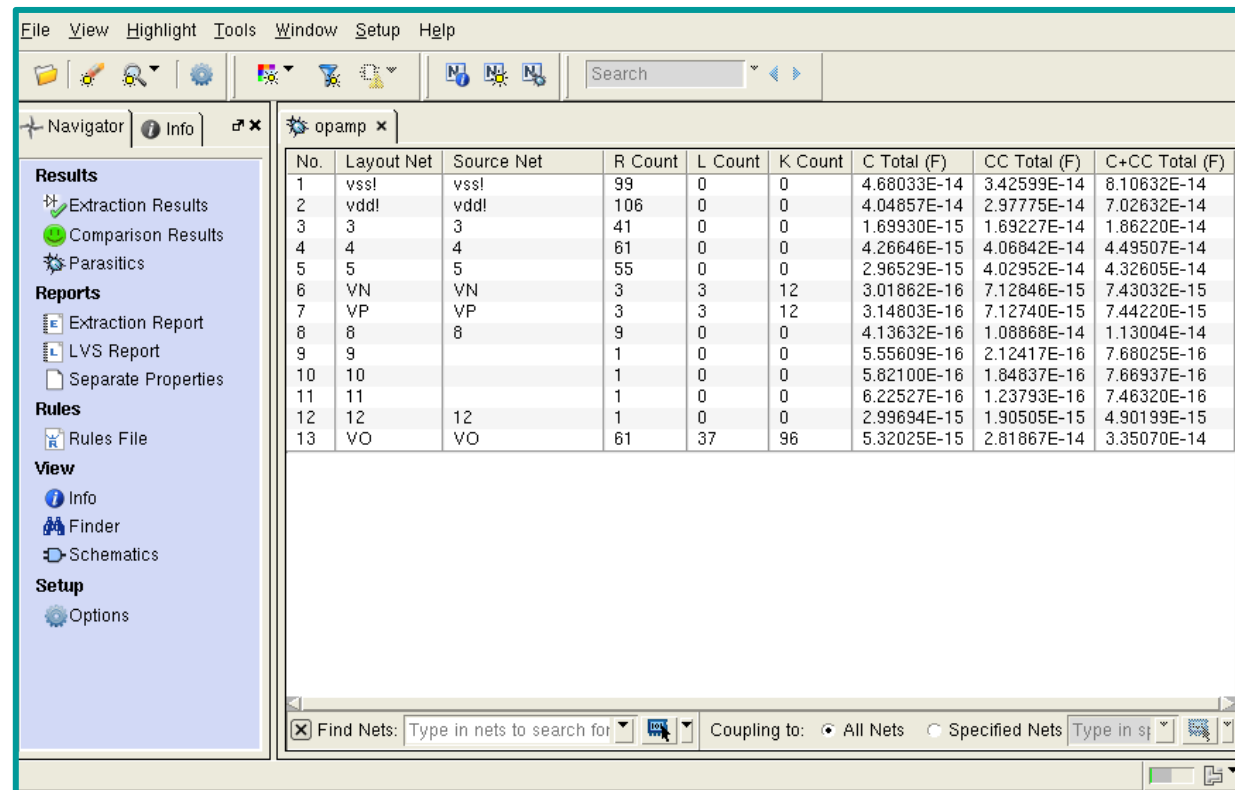
Directions

>> Results PEEC mode

- From the terminal, invoke Calibre RVE with the svdb created from the **PEEC** mode run:

```
calibre -rve PEEC/svdb.PEEC
```

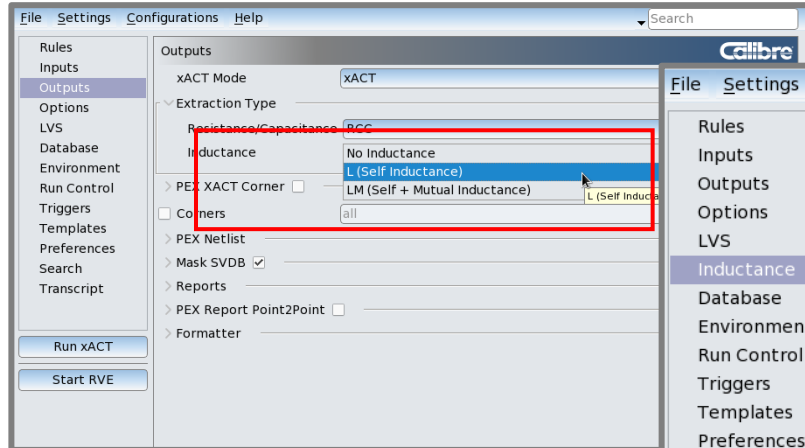
- Notice The Following:
 - Parasitic Inductance for the specified nets only is extracted, including self and mutual inductances
 - Parasitic caps are extracted for all nets



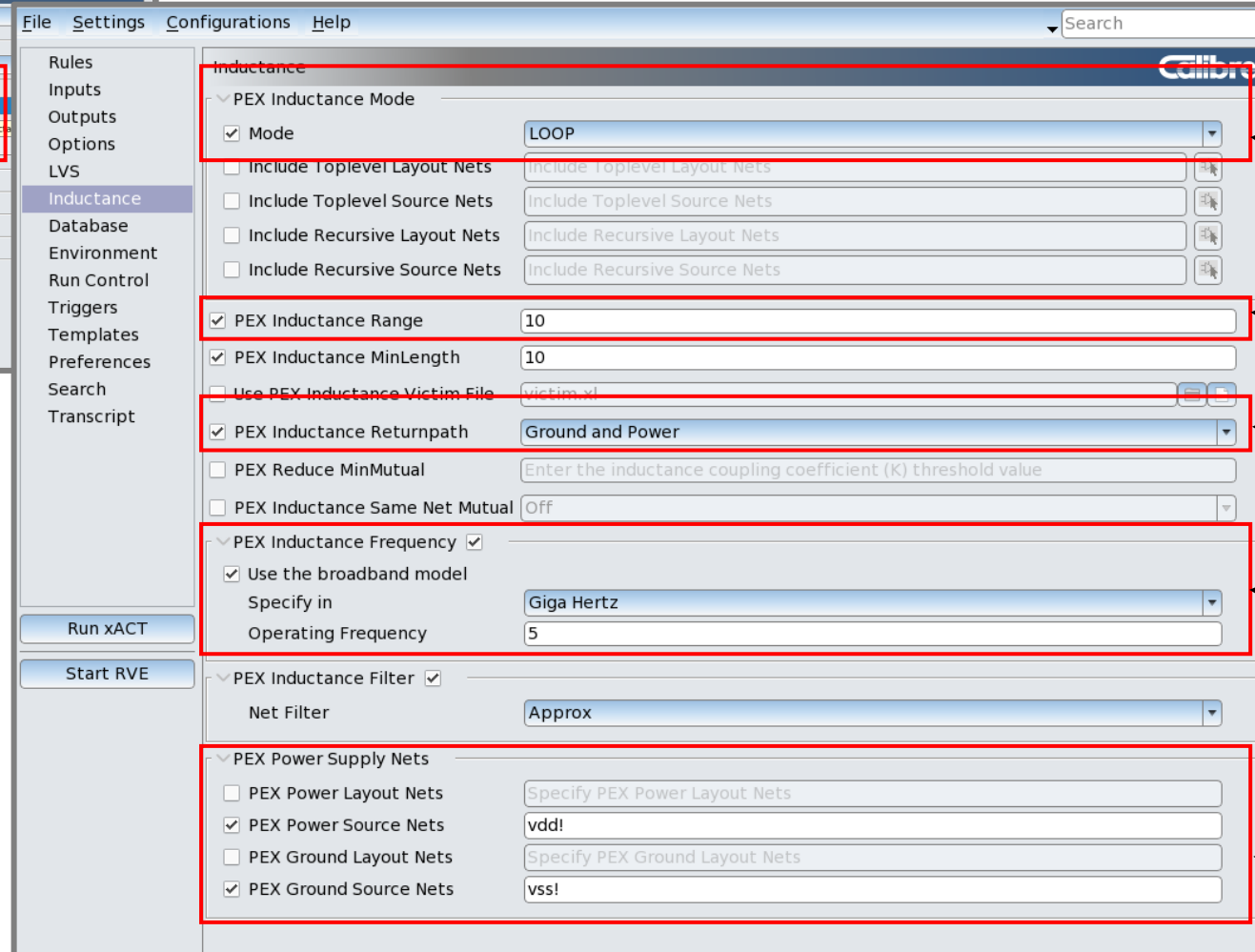
No.	Layout Net	Source Net	R Count	L Count	K Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	vss!	vss!	99	0	0	4.68033E-14	3.42599E-14	8.10632E-14
2	vddl	vddl	106	0	0	4.04857E-14	2.97775E-14	7.02632E-14
3	3	3	41	0	0	1.69930E-15	1.69227E-14	1.86220E-14
4	4	4	61	0	0	4.26646E-15	4.06842E-14	4.49507E-14
5	5	5	55	0	0	2.96529E-15	4.02952E-14	4.32605E-14
6	VN	VN	3	3	12	3.01862E-16	7.12846E-15	7.43032E-15
7	VP	VP	3	3	12	3.14803E-16	7.12740E-15	7.44220E-15
8	8	8	9	0	0	4.13632E-16	1.08868E-14	1.13004E-14
9	9		1	0	0	5.55609E-16	2.12417E-16	7.68025E-16
10	10		1	0	0	5.82100E-16	1.84837E-16	7.66937E-16
11	11		1	0	0	6.22527E-16	1.23793E-16	7.46320E-16
12	12	12	1	0	0	2.99694E-15	1.90505E-15	4.90199E-15
13	VO	VO	61	37	96	5.32025E-15	2.81867E-14	3.35070E-14

Mutual inductance is by default calculated for the selected nets that were specified for the PEEC run

How to Setup the LOOP inductance mode in Calibre xACT GUI



From the "Outputs" tab:
• Select your Inductance



From the "Inductance" tab:

Select your Inductance mode to LOOP

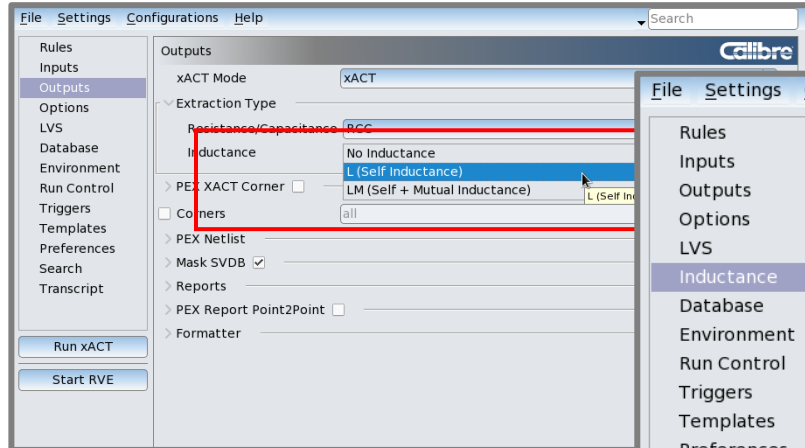
Specify your Inductance range

Specify the returnpath nets

Specify your frequency

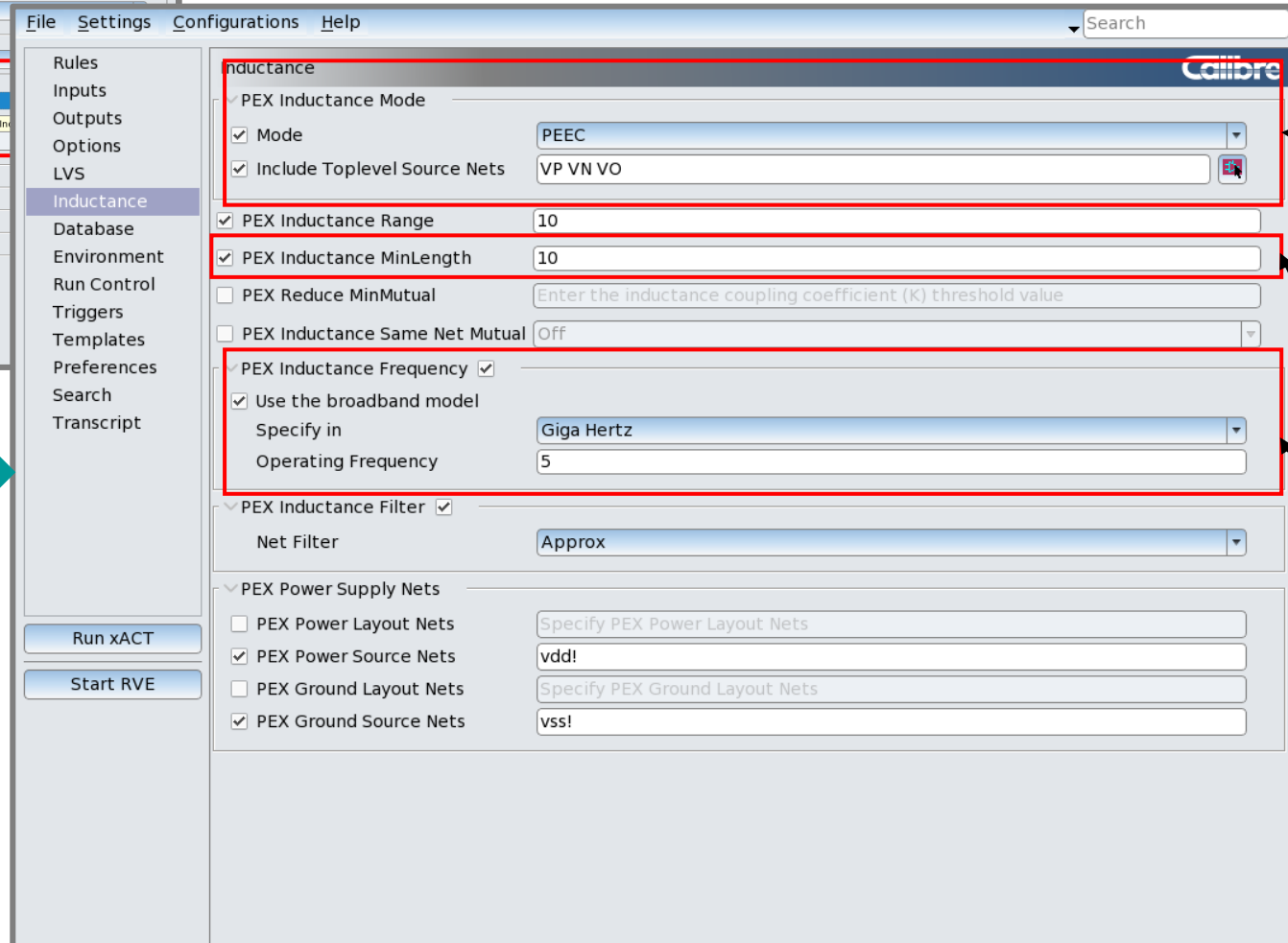
Specify your power and ground nets

How to Setup the PEEC inductance mode in Calibre xACT GUI



From the "Outputs" tab:

- Select your Inductance



From the "Inductance" tab:
Select your Inductance mode to PEEC and include the target nets for inductance extraction

Optional filtering based on signet net length for both LOOP/PEEC (default is 100um)

Specify your frequency. Broadband model specification is ignored in PEEC mode(not supported)

Inductance range settings, returnpath nets and power and ground nets settings are all ignored in PEEC mode

Conclusion



- Ignoring interconnect inductance extraction in analog and RC designs can be a fatal error. With frequency ranges for 5G communication exceeding 40Ghz, designers must ensure that their designs take into account post-layout resistance, capacitance, and inductance parasitics to confirm design simulation results match the silicon-fabricated results.
- Calibre® xL provides a fast, accurate field solver-based inductance extraction engine to extract both self and mutual inductance parasitics of on-chip interconnects.
- Calibre® xL can be easily streamlined in the verification flow since is fully integrated with Calibre® xRC™, Calibre® xACT™ & Calibre® xACT3D™ . It offers various features including selected net extraction, customizable return path selection, and net-by-net frequency selection.
- Please refer to the **Standard Verification Rule Format (SVRF) Manual, Calibre® xACT™ User's Manual and Calibre® xRC™ User's Manual** for additional information.

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